Optical Interconnection Architecture for On-Board Multi-Chip System

Abstract:

Incorporating optics in close proximity to high-performance electronic chips on the board-level can not only allow substitution of the existing electrical connections with faster, more power-efficient alternatives, but most importantly, the radical re-design of the system architecture and yet has had limited exploration. Performance of optical links have interdependence on the link utilisation by the application traffic, which makes optical design space a multi-dimensional challenge. We need a solution that looks at the problem from different perspectives, and considers all aspects including the allocation of system resources, technologies and network topology for different applications. Through our study we want to develop a tool that can help in quantifying these design trade-offs, which will in turn help us in designing optimal architectures functioning with high bandwidth, energy efficient optical links. In this project therefore, we study various board-level interconnection architectures for multiple computing chips using on-board optics taking into account recent achievements in the field. To conduct a performance metric simulation, we input our designs into an architecture simulator in combination of an opto-electronic device modelling tool and run for standard workload benchmarks. We compare our design trade-offs with respect to each architecture based on the different available technologies and derive the optimum configuration for execution time, power consumption and implementation complexity.