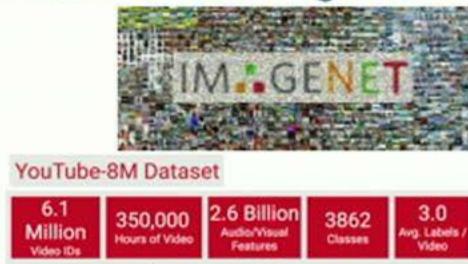
# Scheduling for Efficient Large-Scale Machine Learning Training

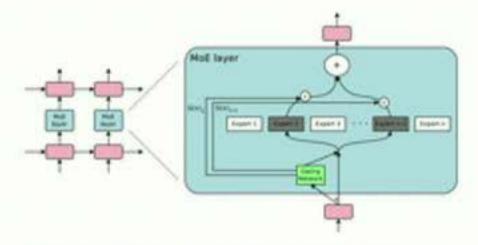
Jinliang Wei Carnegie Mellon University



# Machine Learning Training: Quest for Efficiency



Growing data size



Growing model complexity

### Challenges:

Machine learning models take long time to train.

Machine learning training consumes large amount of memory.

Implementing parallel/distributed programs is hard.

### Key Idea:

Leverage general structural properties in ML computation to improve efficiency

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### Challenges:

What structural properties are helpful?

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How to leverage it with no / little burden to users?

### Key Idea:

Leverage general structural properties in ML computation to improve efficiency



### Systems developed:

Bösen: (parameter server) [SoCC'15] ~20K LoC (C++)

Orion: (auto-parallelization) [EuroSys'19] ~23K LoC (C++, Julia)

Non-trivial work on TensorFlow core

### Challenges:

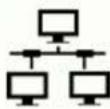
What structural properties are helpful?

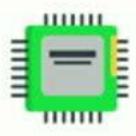
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# Scheduling within a Single Training Job

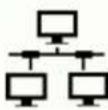
# Scheduling within a Single Training Job







## Scheduling within a Single Training Job

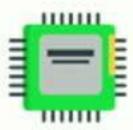


**Network Communication** 

When and what to send?

Lead [SoCC'15, Best paper]

Coauthor [ATC'17] [SysML'19]



Computation

What to compute in parallel?

[EuroSys'19]



Memory Allocation

When and where to allocate?

[In preparation]

### Highlights of results:

- Scheduling communication: up to 30% faster convergence
- Scheduling computation: even faster convergence with less programmer effort
- Scheduling memory: 10x bigger model on the same hardware

Sequential learning algorithm, e.g., SGD:

repeat until convergence foreach mini-batch in dataset update model parameters

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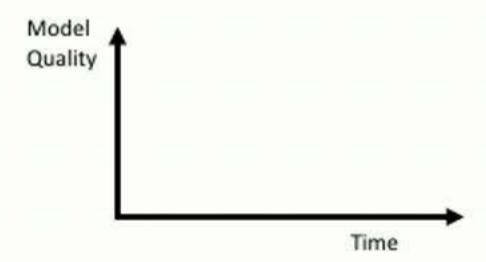
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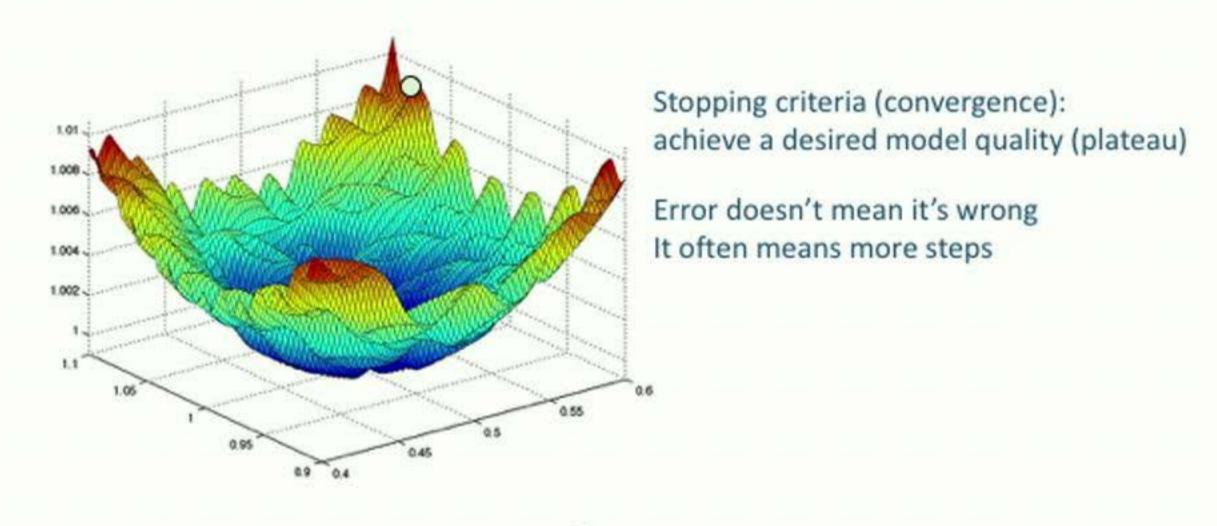
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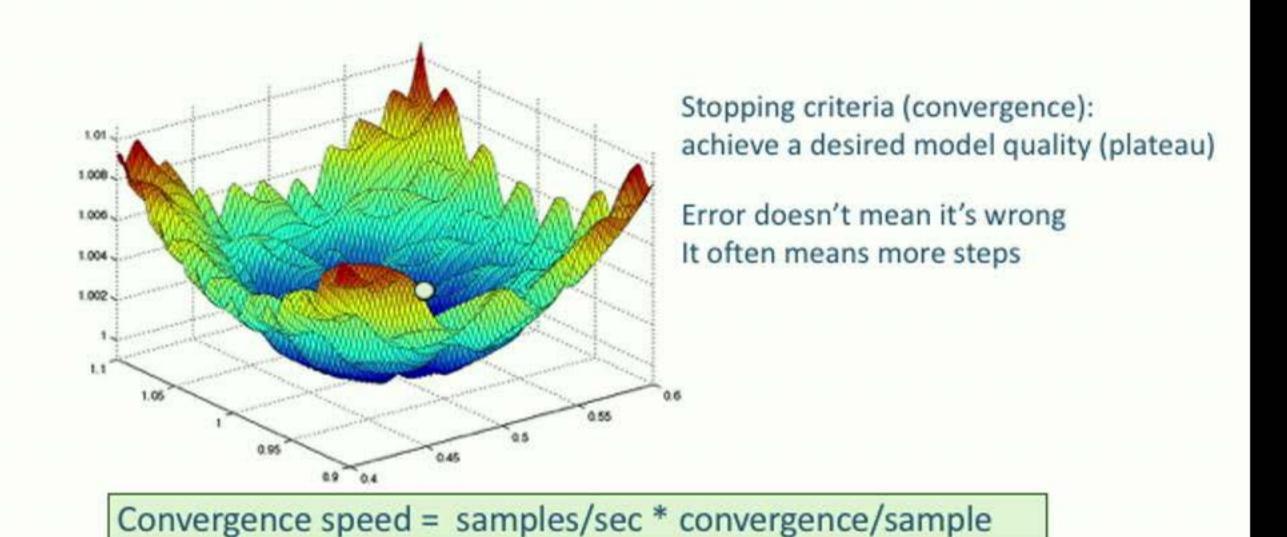
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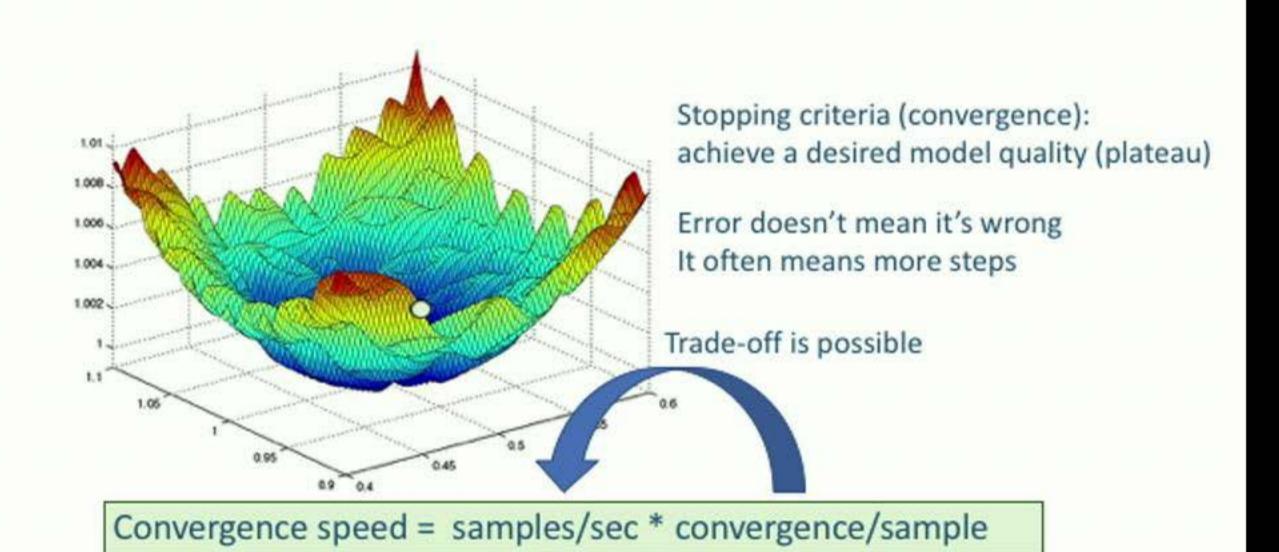
## Machine Learning Training Is A Search Process



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### Background: Data Parallelism for Computation Throughput

Simply run some / all mini-batches in parallel, regardless of dependence

repeat until convergence
in parallel foreach mini-batch in dataset
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Parameter Server

Workers

Convergence speed = samples/sec X convergence/sample

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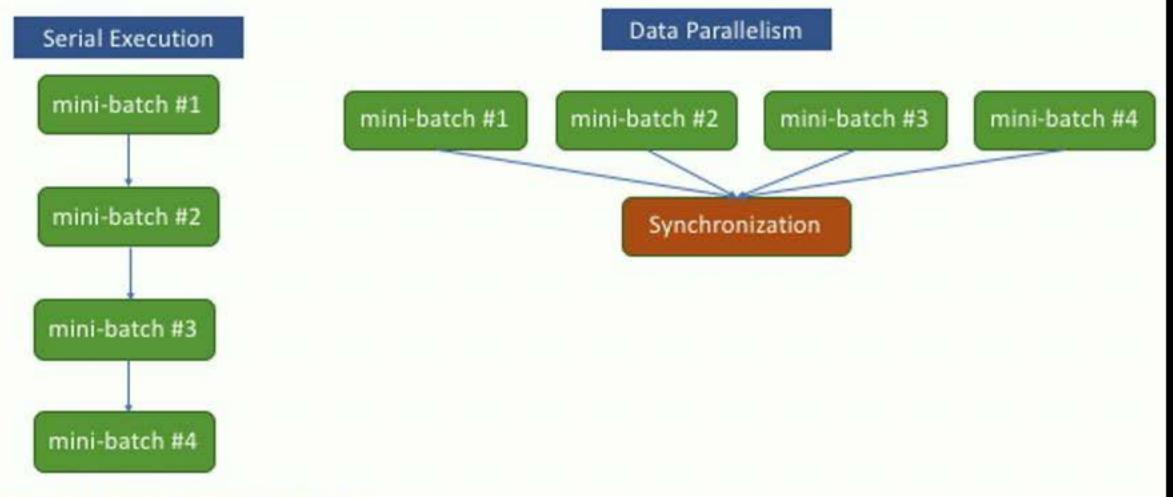
Serial Execution

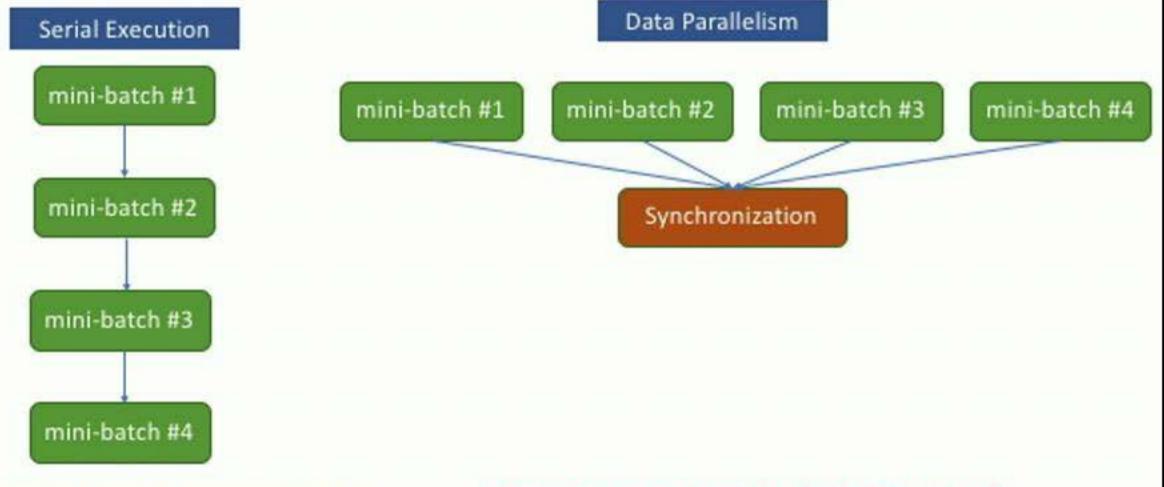
mini-batch #1



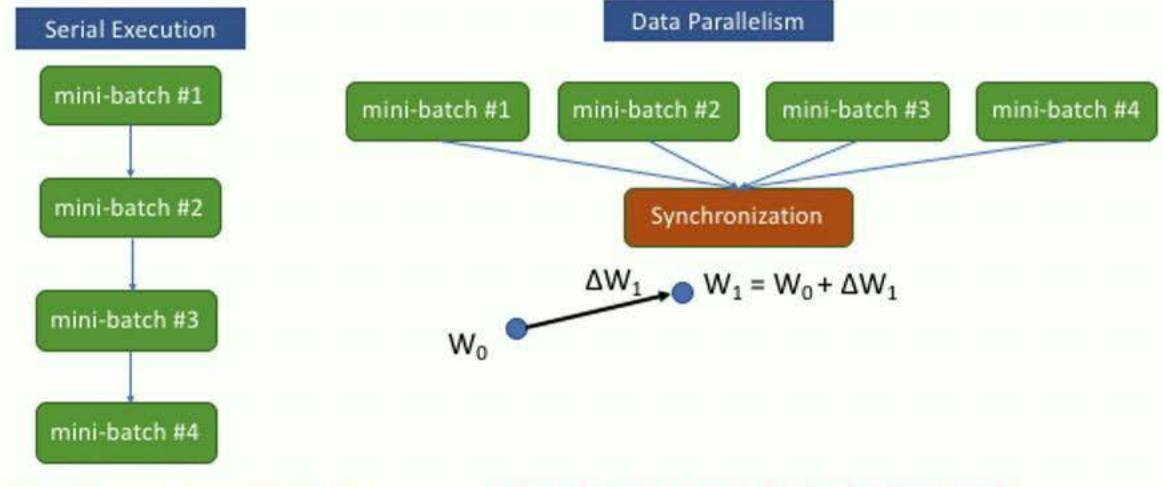




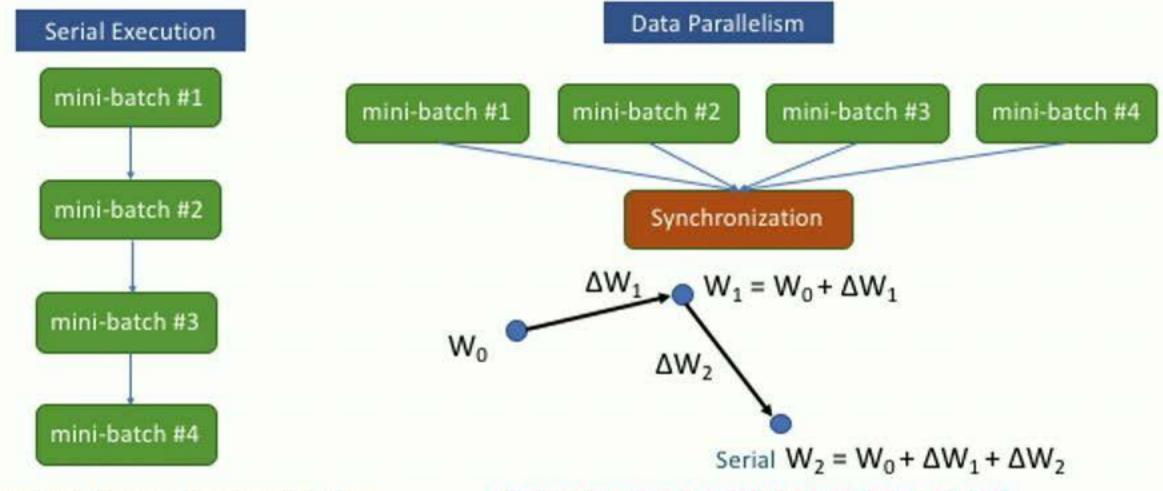




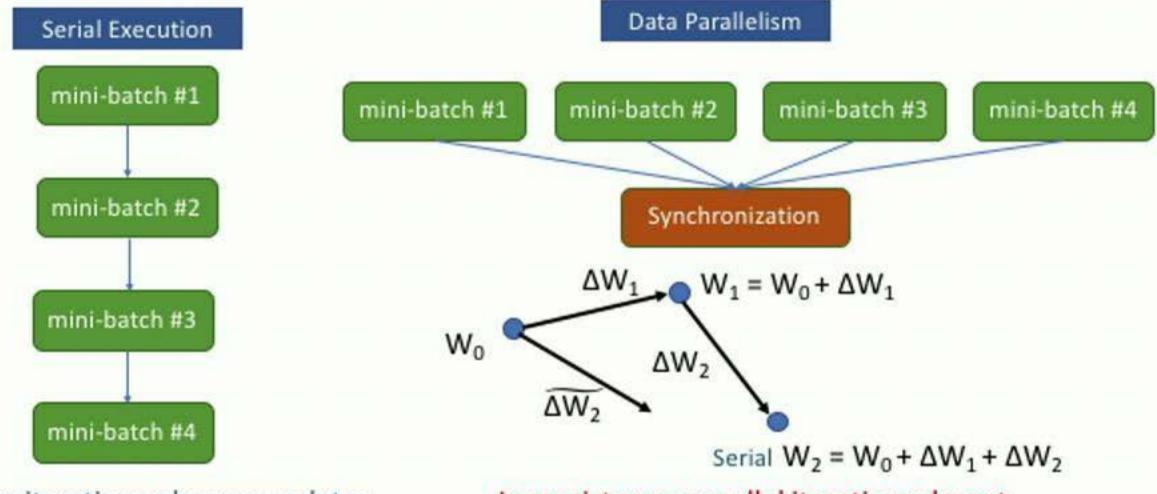
Later iterations observe updates from earlier iterations



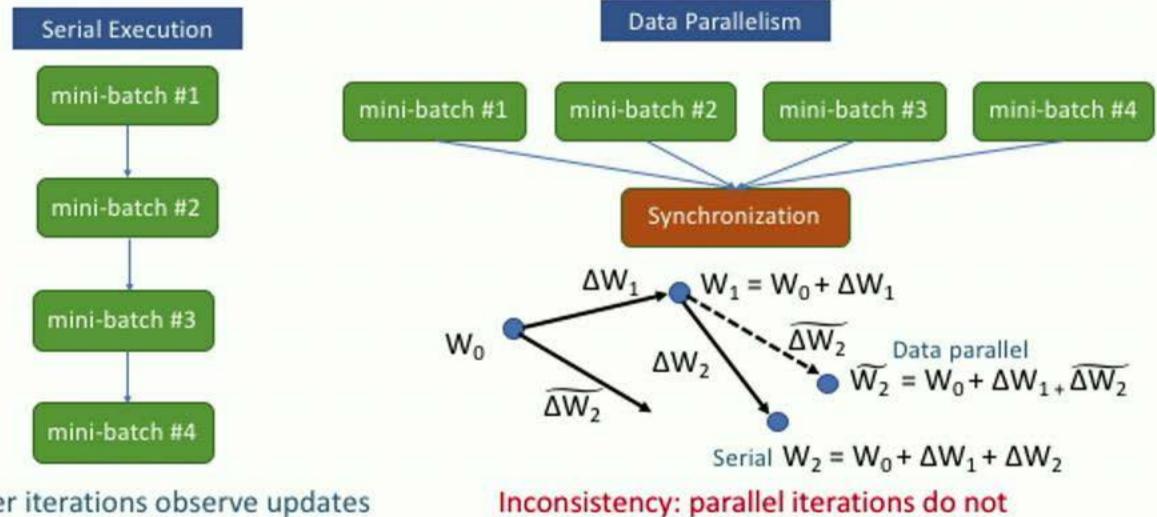
Later iterations observe updates from earlier iterations



Later iterations observe updates from earlier iterations



Later iterations observe updates from earlier iterations



observe updates from each other

### Background: Sparsity and The Communication Bottleneck

ML models of interest (5~10 years ago): Simple and highly sparse

Sparse Logistic Regression Latent Dirichlet Allocation (LDA) Matrix Factorization (MF) ...

### Problem:

Light computation per mini-batch vs. heavy communication

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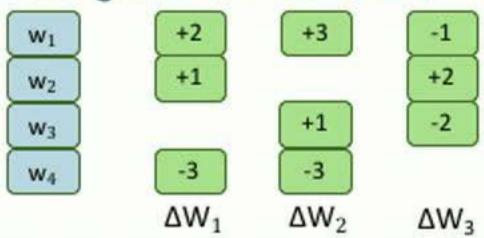
Compute

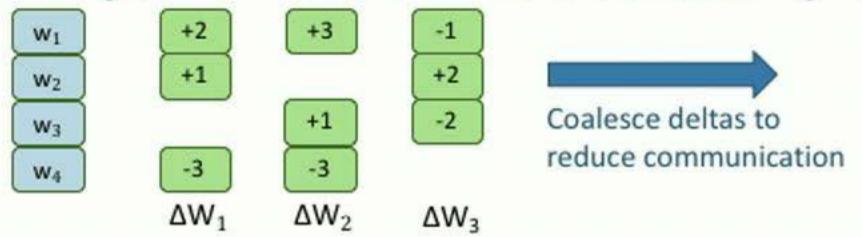
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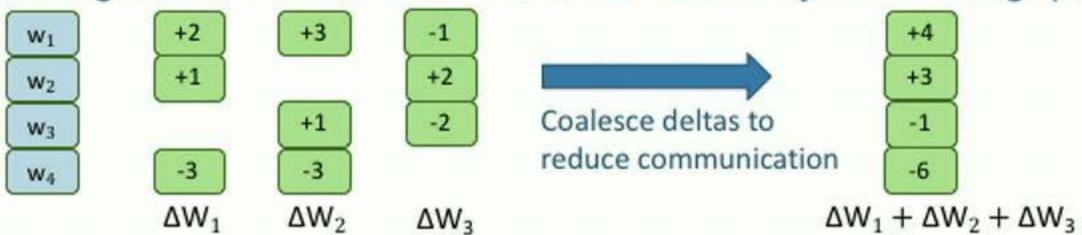
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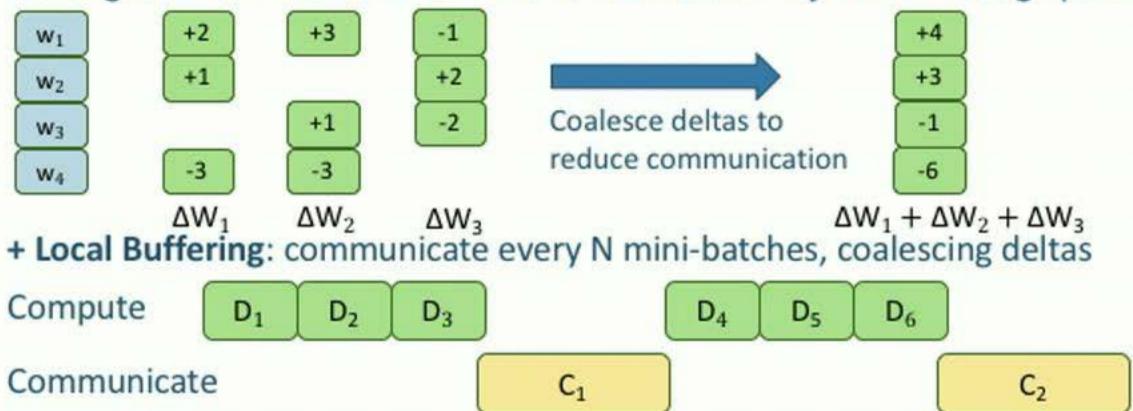
# Problem:Light computation per mini-batch vs. heavy communicationCompute $D_1$ $D_2$ $D_3$ Communicate $C_1$ $C_2$ $C_3$

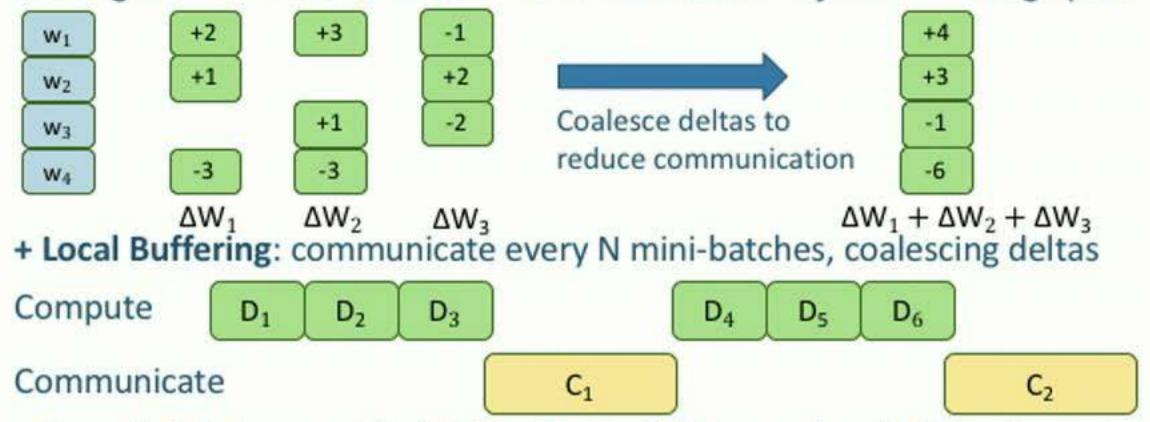
# Background: Trade Even More Consistency for Throughput



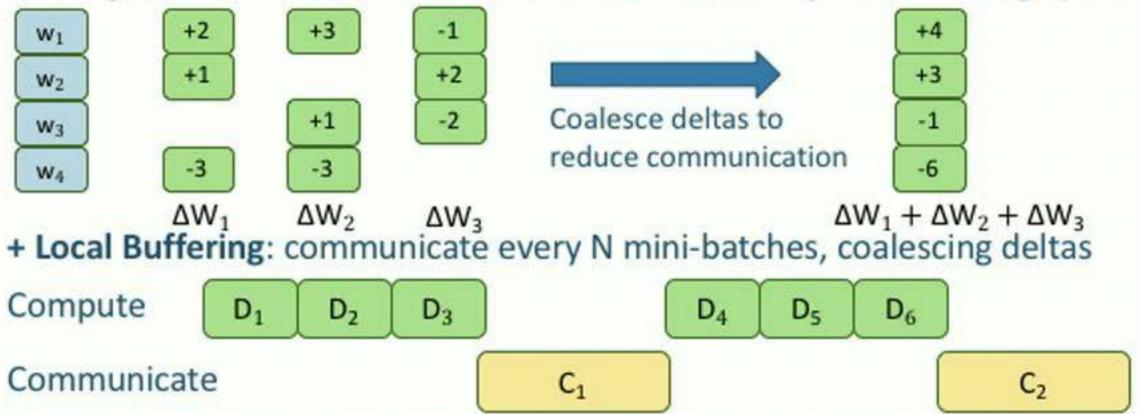




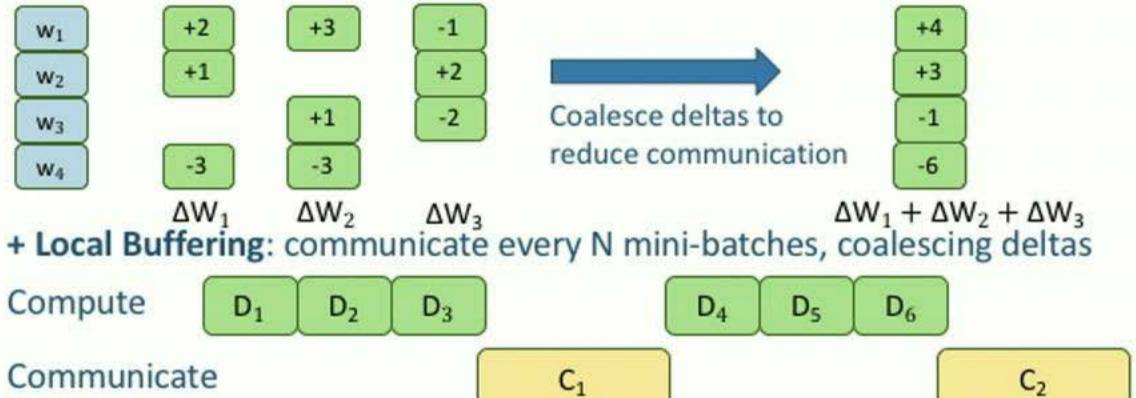




+ Bounded Staleness: block iff the fastest is T steps ahead of the slowest

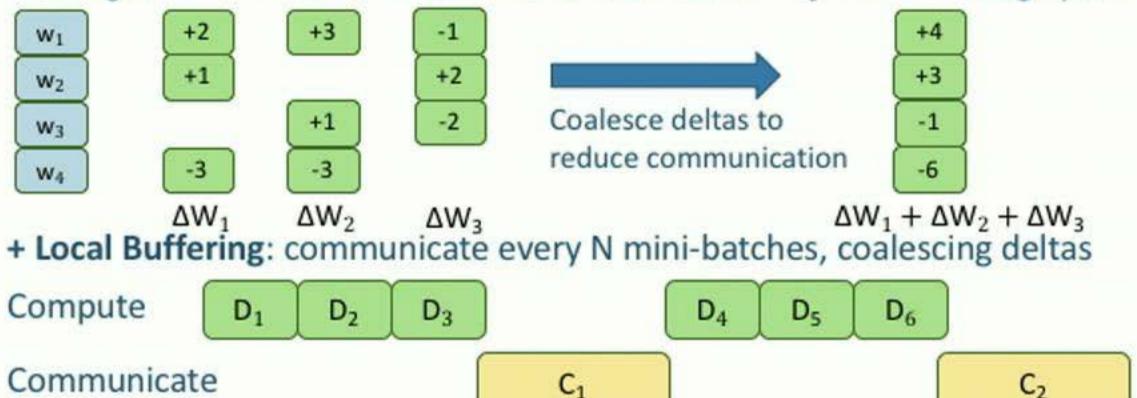


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Compute D<sub>1</sub> D<sub>2</sub> D<sub>3</sub>

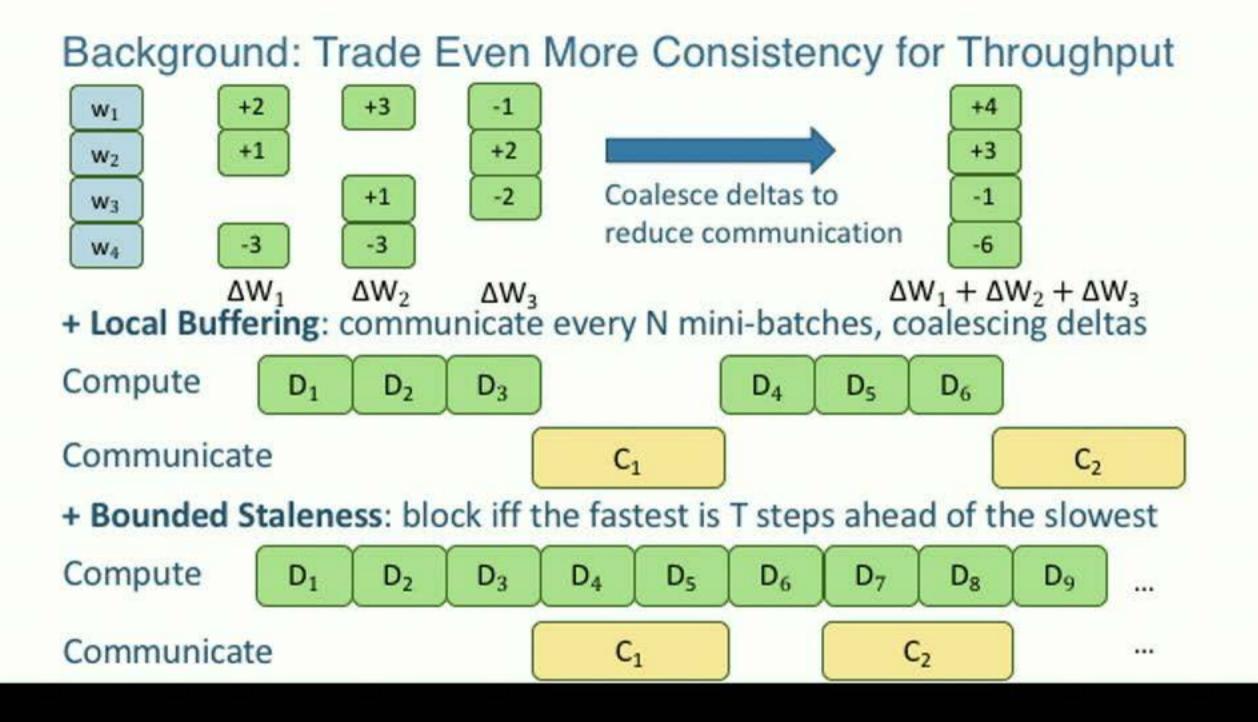


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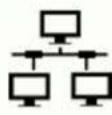
Compute  $D_1$   $D_2$   $D_3$ 

Communicate

#### Background: Trade Even More Consistency for Throughput +4 WI +3 +1 W2 Coalesce deltas to -1 +1 W3 reduce communication -3 -6 W4 $\Delta W_1 + \Delta W_2 + \Delta W_3$ $\Delta W_1$ $\Delta W_2$ $\Delta W_3$ + Local Buffering: communicate every N mini-batches, coalescing deltas Compute $D_6$ $D_1$ $D_2$ $D_3$ Ds Communicate $C_1$ C, + Bounded Staleness: block iff the fastest is T steps ahead of the slowest Compute D2 $D_6$ $D_3$ Communicate



#### Reduce Inconsistency via Scheduling



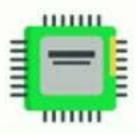
**Network Communication** 

When and what to send?

Publication [SoCC'15, Best paper]

Systems Developed

Bösen: parameter server



Computation

What to compute in parallel?

[EuroSys'19]

Orion: parallelization framework

#### Highlights of results:

- Scheduling communication: up to 30% faster convergence
- Scheduling computation: even faster convergence with less programmer effort

Data parallelism, + local buffering + bounded staleness:

Compute  $D_1$   $D_2$   $D_3$   $D_4$   $D_5$   $D_6$   $D_7$   $D_8$   $D_9$  ...

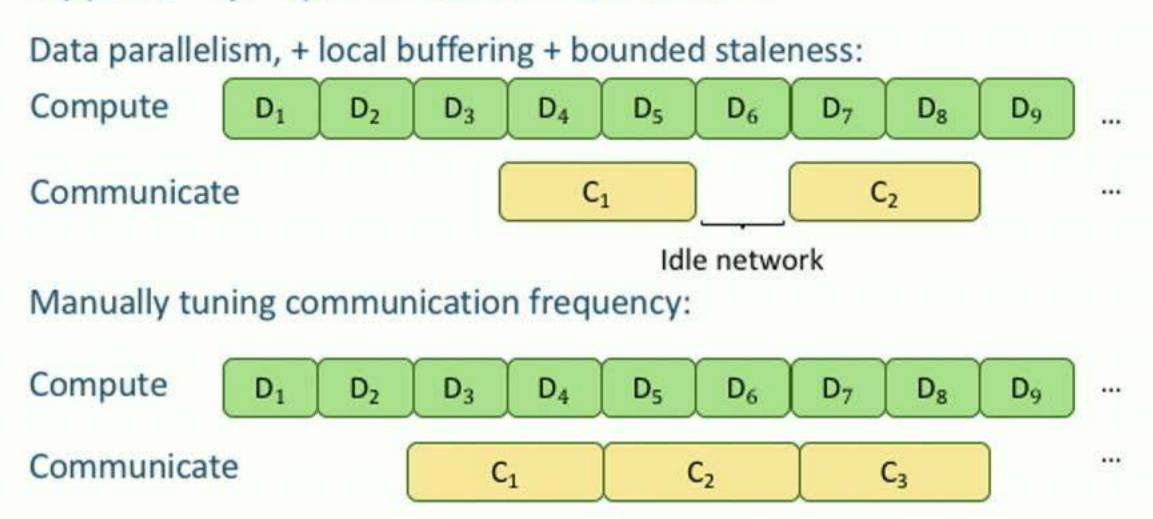
Communicate  $C_1$   $C_2$  ...

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Idle network



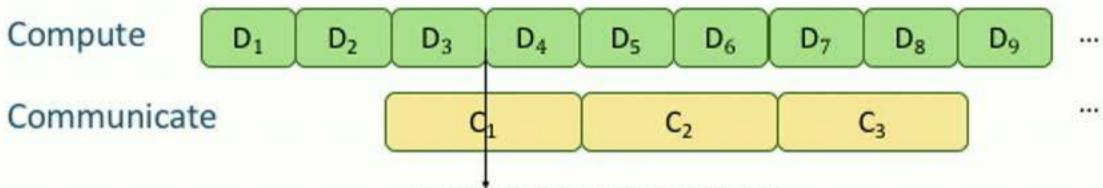
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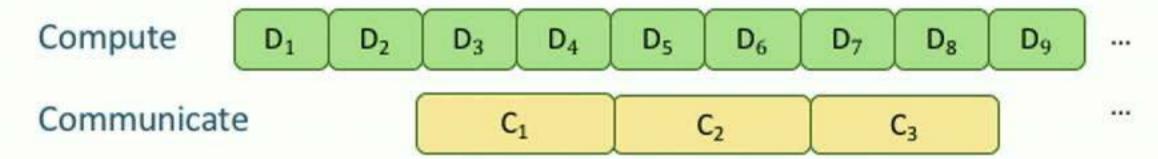
Idle network

Manually tuning communication frequency:



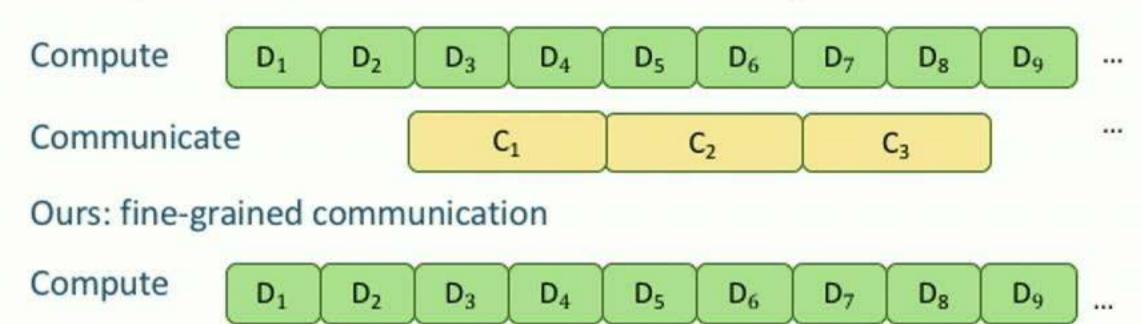
D<sub>3</sub> updates become available, more effective to communicate coalesced updates

Existing: manually tuned communication frequency

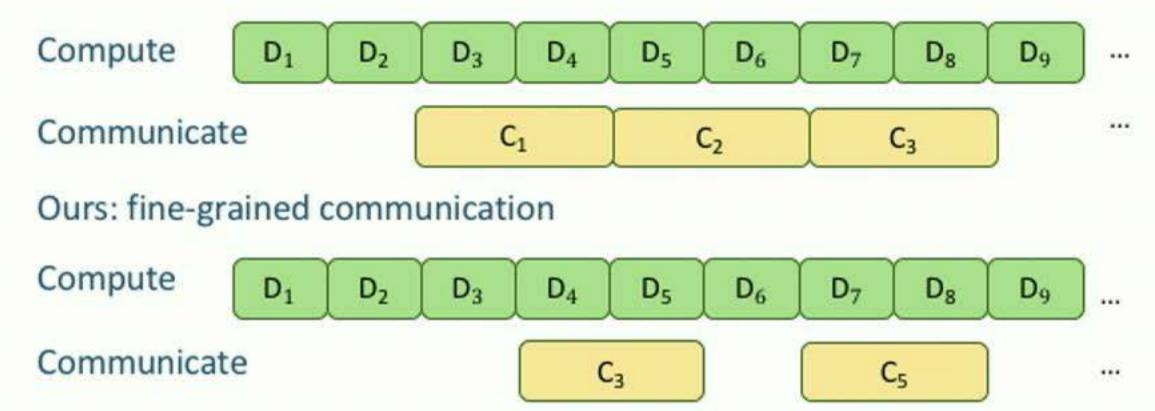


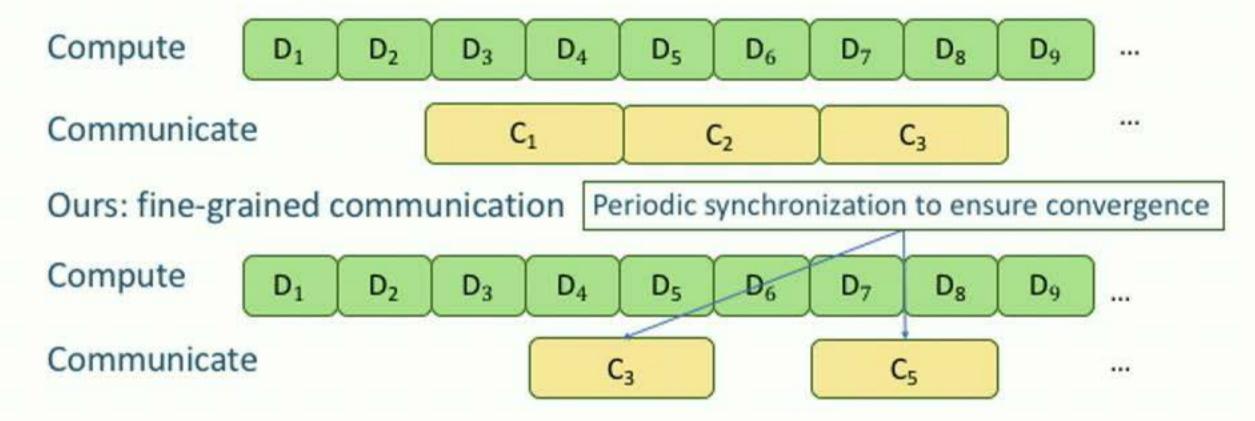
...

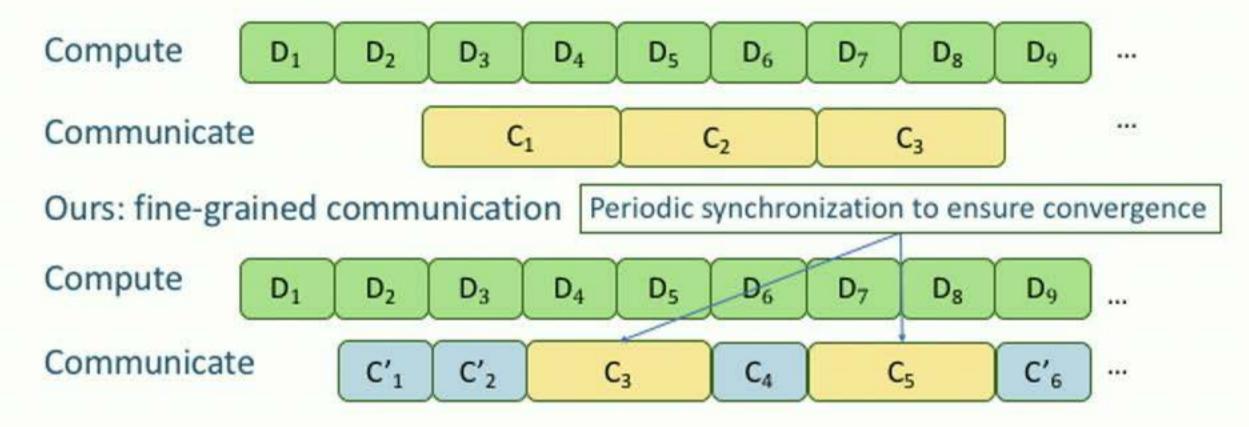
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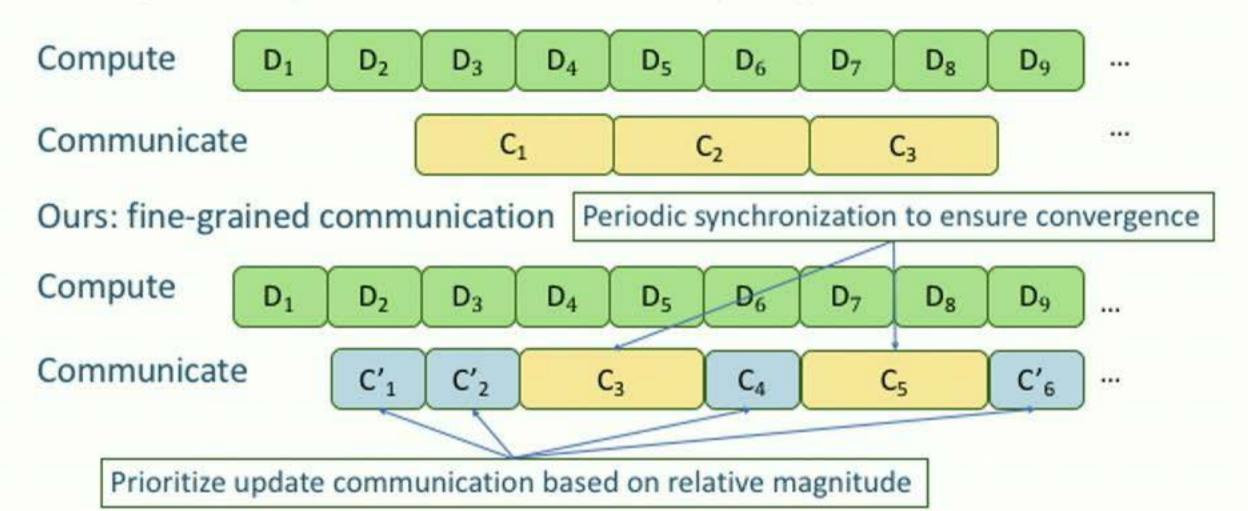


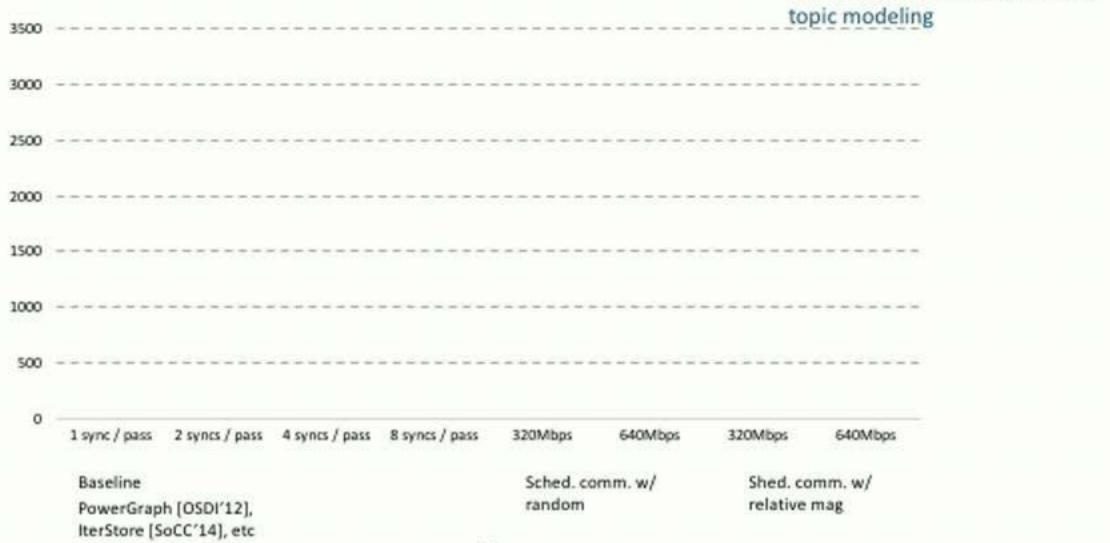
Communicate ...



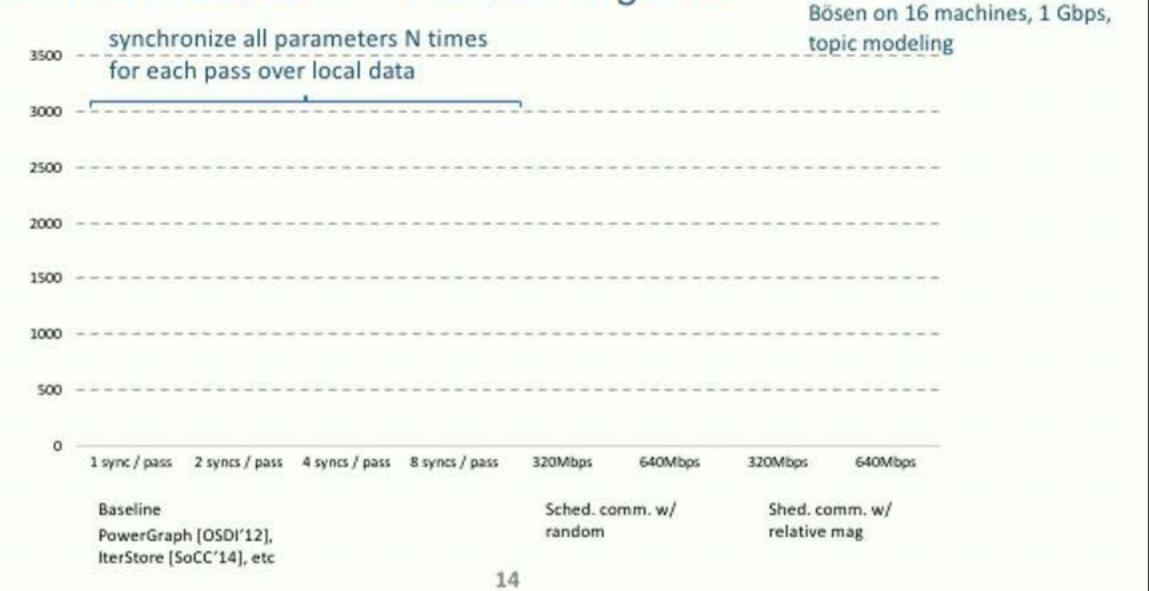


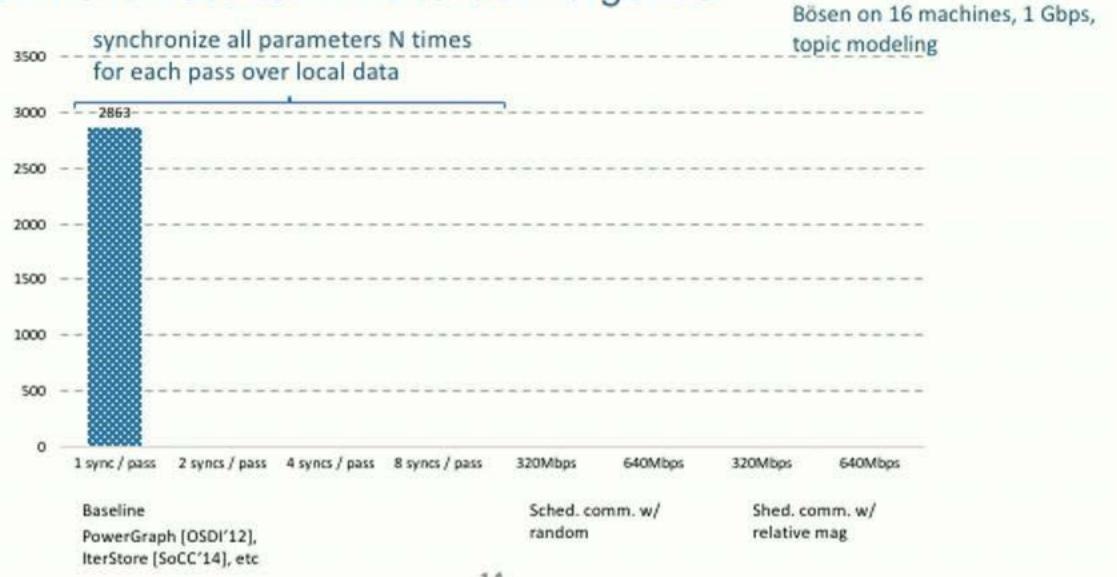


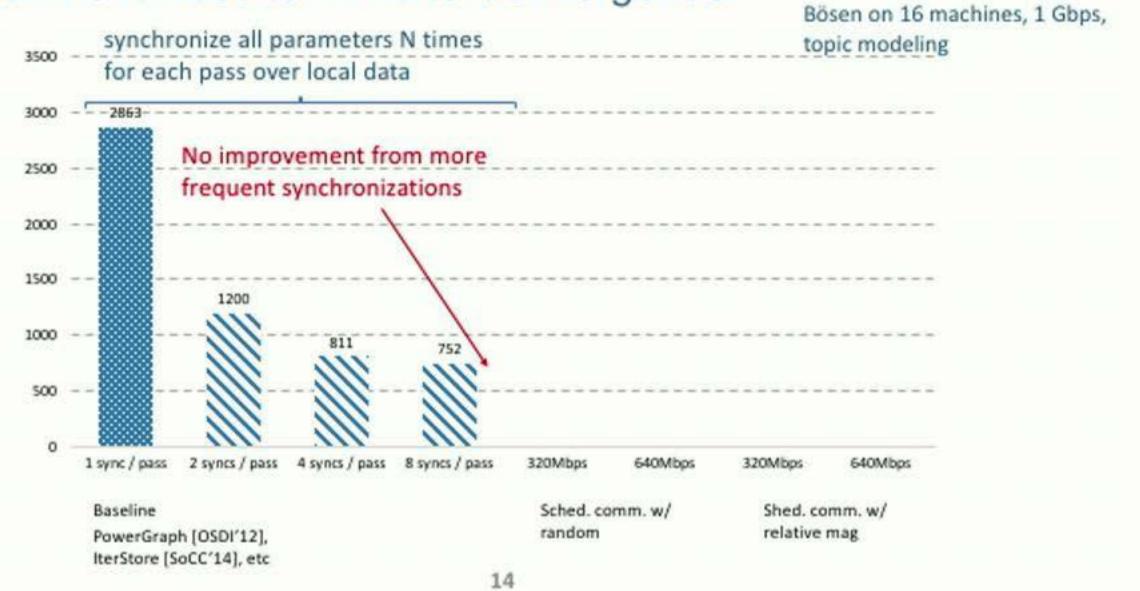


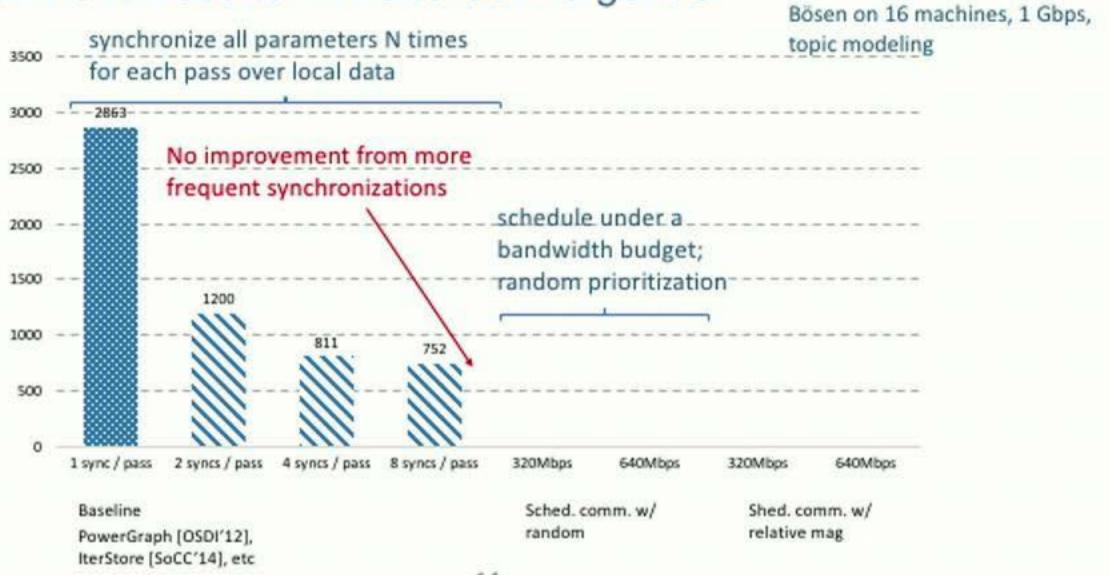


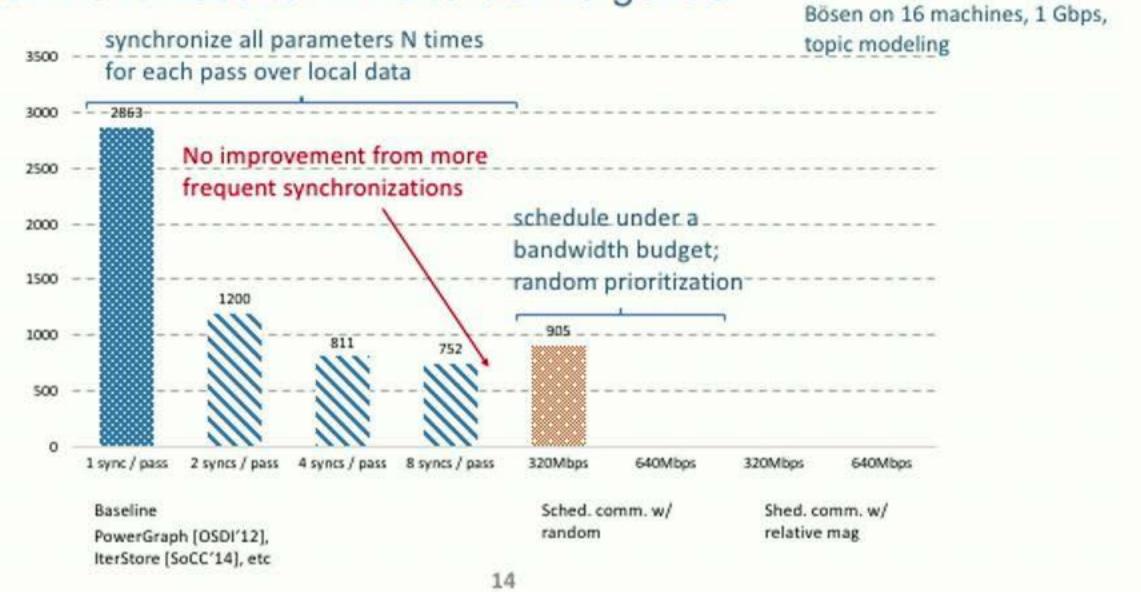
Bösen on 16 machines, 1 Gbps,

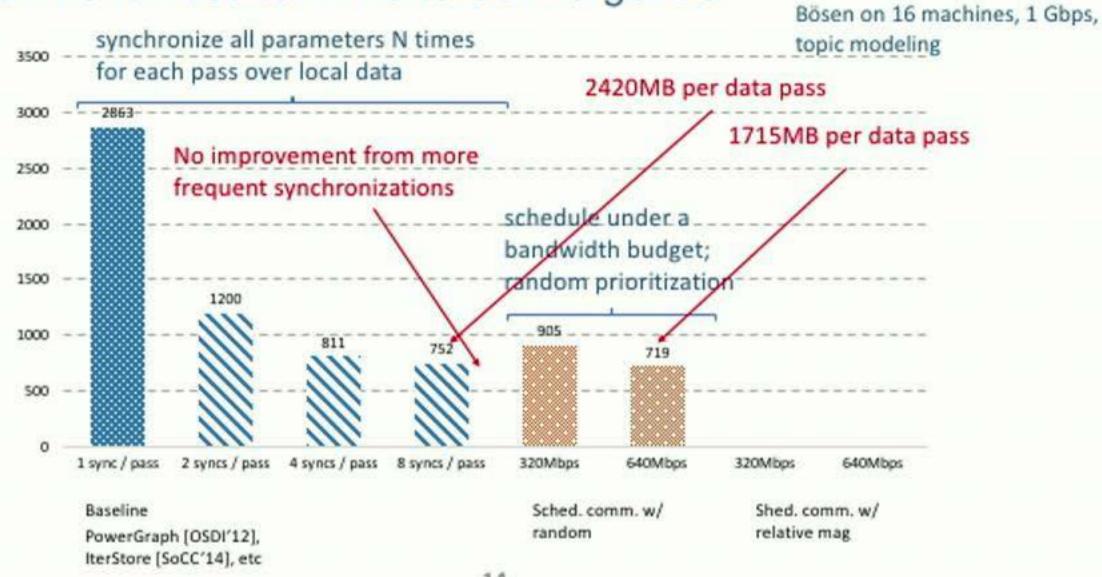


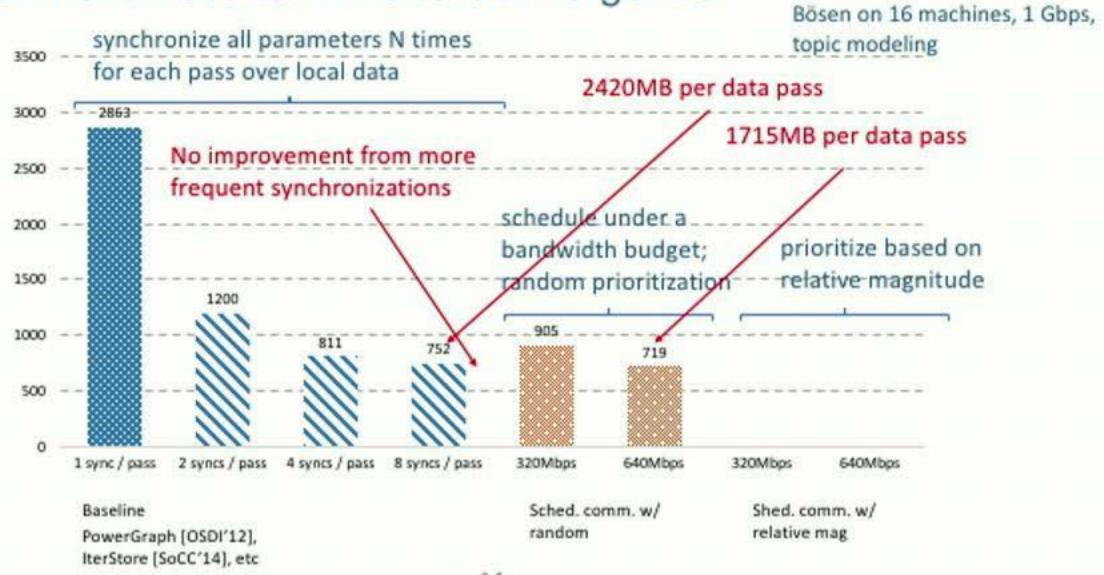


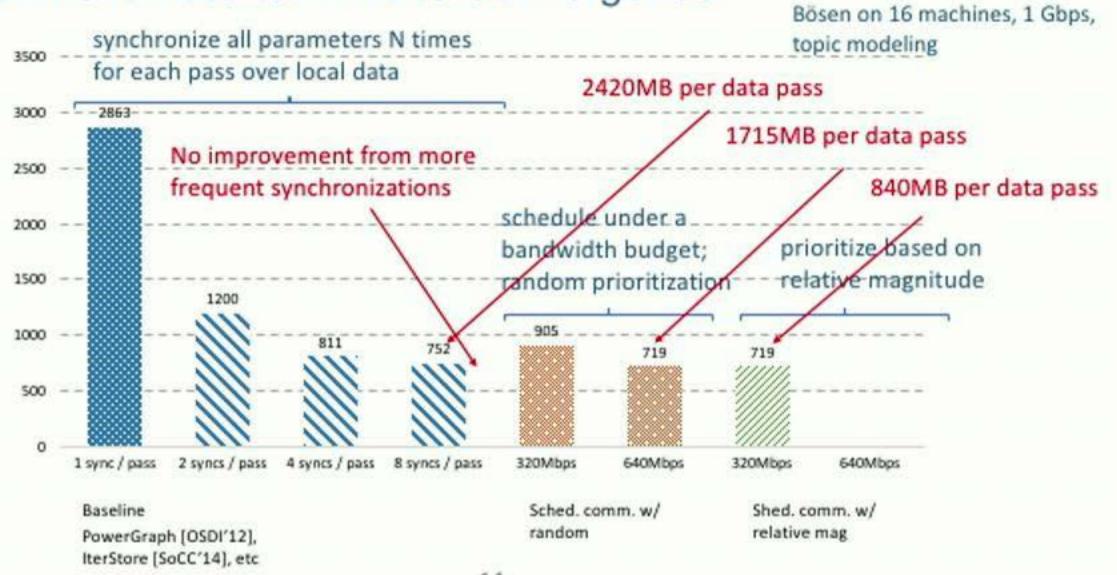


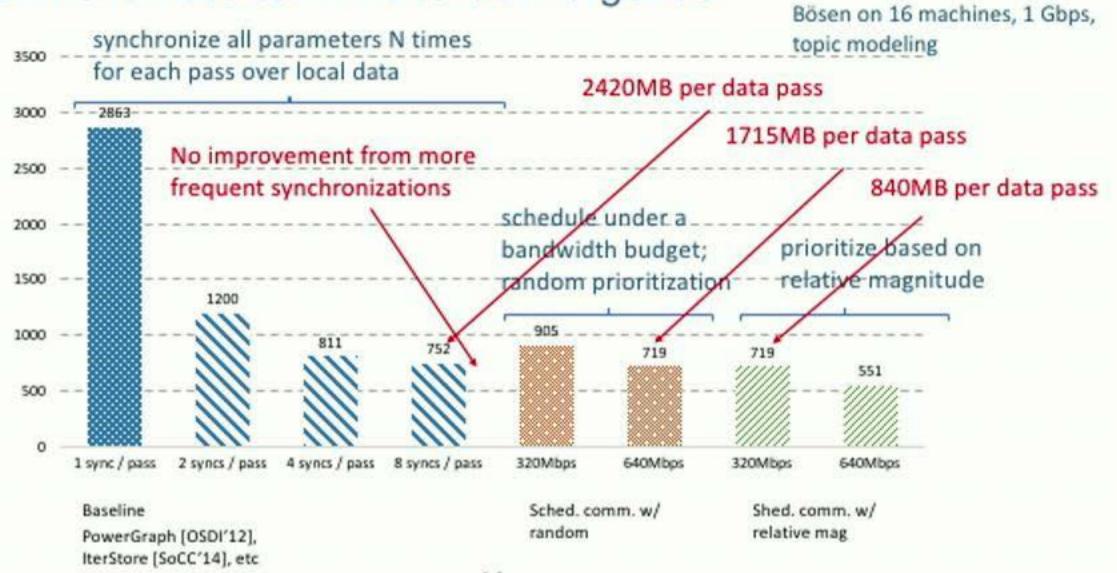








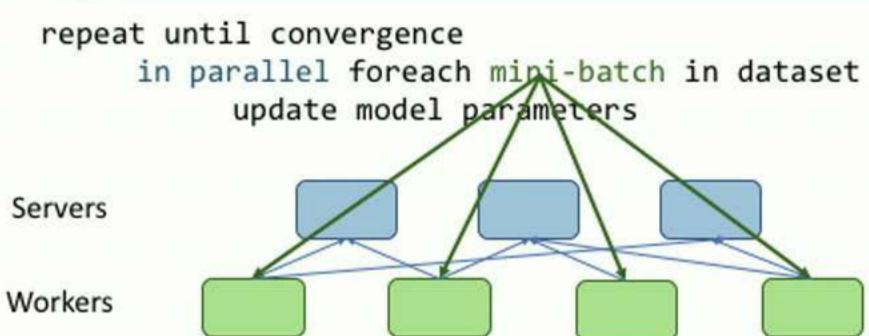




#### Schedule Computation To Reduce Inconsistency



#### Execute only independent mini-batches in parallel



#### Structural Sparse Parameter Access In ML

In some models, parameters are accessed based on data sample attributes.

Example:

Model: Matrix Factorization

Application: Recommender systems

Parameters: User Latent Vectors

**Item Latent Vectors** 

#### Data sample:

UserID	ItemID	Rating
#38	#65	5.0

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Other examples: topic modeling, gradient boosted trees, etc.

#### Partition The Dataset for Nonconflicting Accesses

```
There exist f_1, f_2, ..., f_k, such that if d_i[f_1] != d_j[f_1], d_i[f_2] != d_j[f_2], ..., and d_i[f_k] != d_j[f_k], d_i and d_j don't access the same parameters.
```

Partition the dataset by those fields

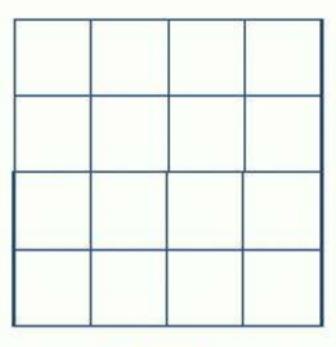


Dataset

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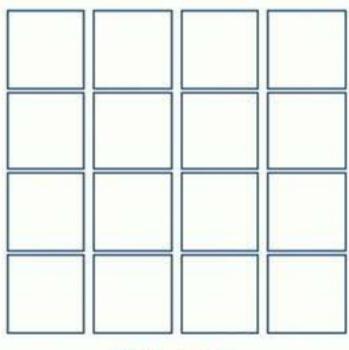


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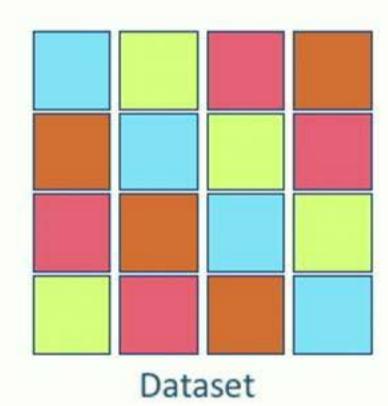


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Nonconflicting parameter accesses



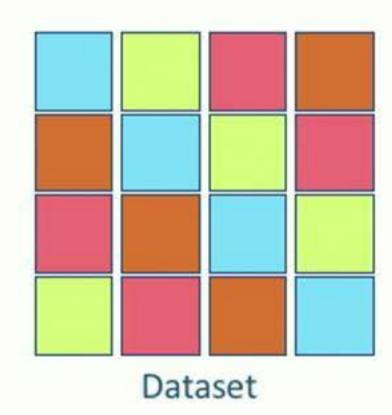
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Partition the dataset by those fields

Nonconflicting parameter accesses

Special case of automatic parallelizing compilers



# Challenges for Scheduling Computation

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Challenge #1: applicable only when certain property holds

Solution: fall back to data parallelism otherwise

### Challenges for Scheduling Computation

Challenge #1: applicable only when certain property holds

Solution: fall back to data parallelism otherwise

Challenge #2: implementation requires non-trivial programmer effort

Solution: automatically parallelize serial programs

## Orion: Automatic Parallelization [Wei, et al., EuroSys'19]



#### Our goals:

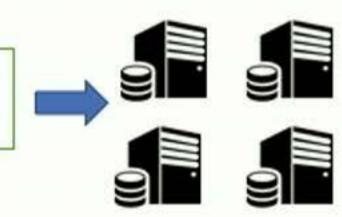
- A parallel\_for construct and users implement a serial program;
- 2. Preserves sequential semantics when possible;
- 3. Data parallelism otherwise with user permission



#### Orion's abstraction:

A single thread w/ huge memory

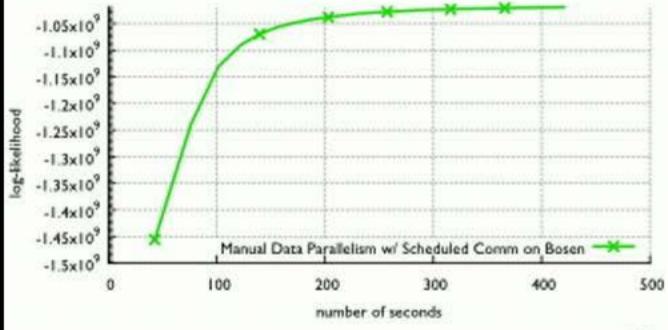
Serial ML program in Julia

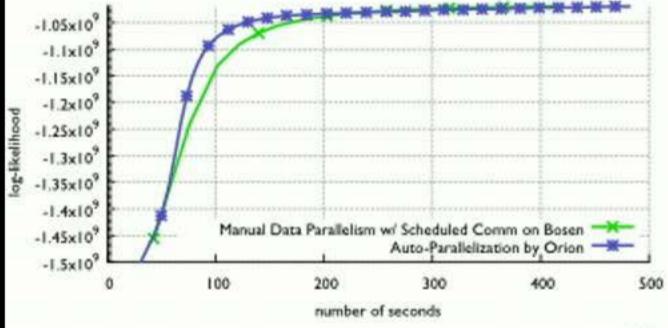


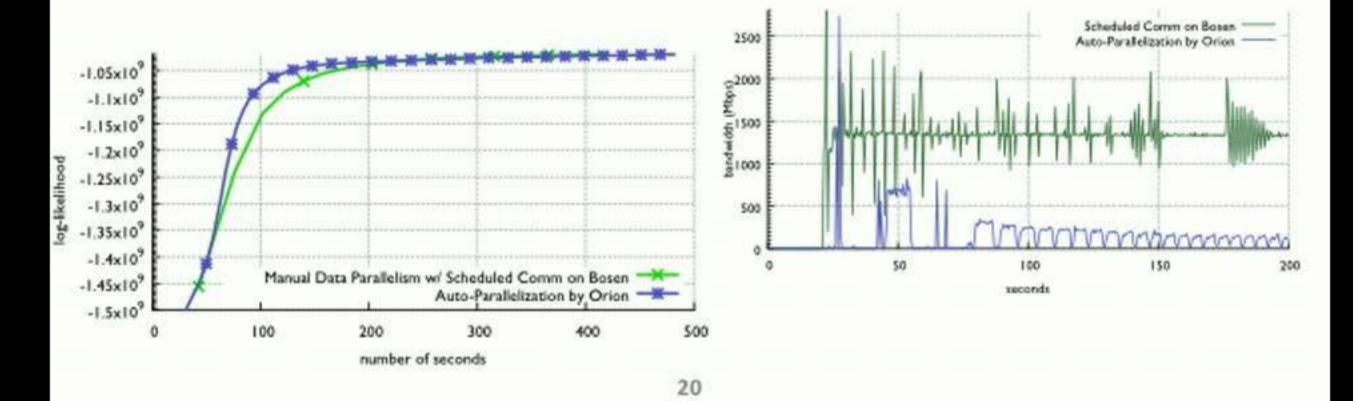
12 machines, 32 vCPU cores / machine

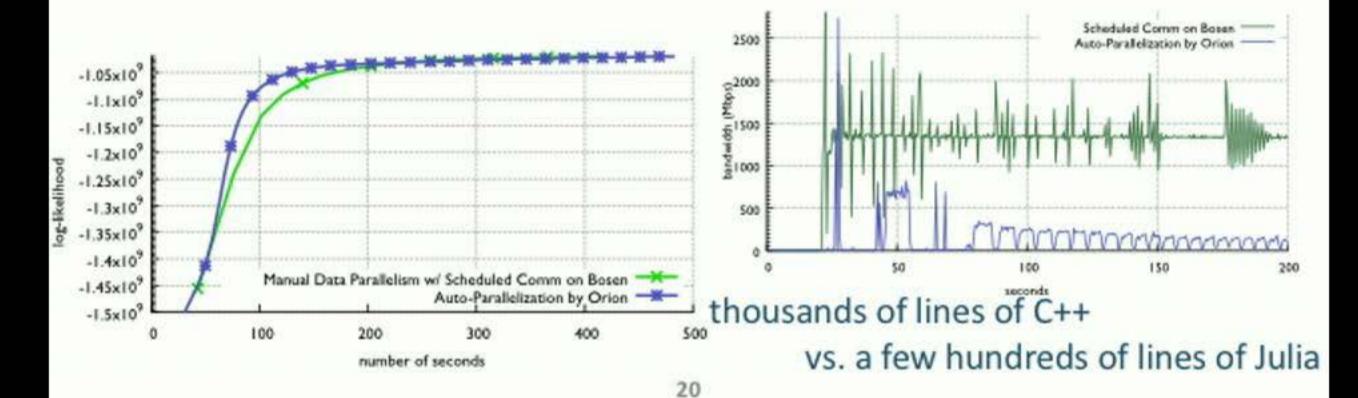
40 Gbps Ethernet

Latent Dirichlet Allocation (LDA) for topic modeling + Gibbs sampling algorithm



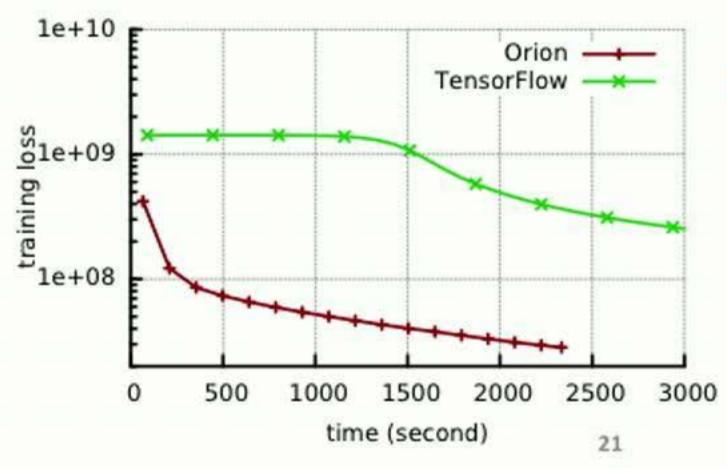






### Compare Orion vs. TensorFlow

1 machines, 32 vCPU cores / machine Matrix Factorization (MF) for recommendations + SGD



TensorFlow suffers due to

- Data parallelism
  - Slower per-sample convergence
- Poor support for sparsity
- 2x longer time per iteration

#### The Developing View: More And More Complex ML Models

```
repeat until convergence

foreach mini-batch in dataset

update model parameters
```

We've focused improving computation across mini-batches.

#### The Machine Learning Trend:

The mini-batch computation is becoming more and more complex

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#### **Deep Neural Networks:**

Heavy computation per mini-batch

Dense parameter access

Synchronize after each mini-batch

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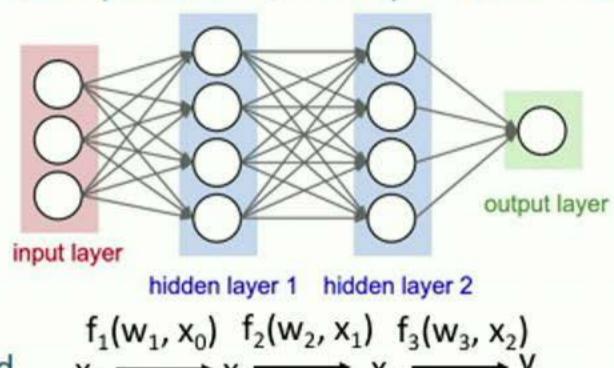
Dense parameter access

Synchronize after each mini-batch

#### Opportunity:

Improve DNN efficiency without scarifying computation quality

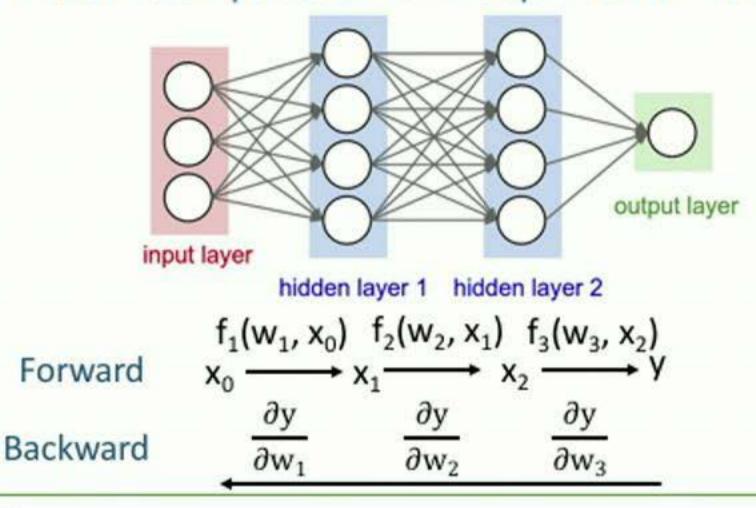
#### The Mini-Batch Computation of Deep Neural Networks



Forward 
$$x_0 \xrightarrow{f_1(w_1, x_0)} f_2(w_2, x_1) f_3(w_3, x_2)$$

$$x_0 \xrightarrow{\partial y} x_1 \xrightarrow{\partial y} x_2 \xrightarrow{\partial y} y$$
Backward  $\frac{\partial y}{\partial w_1} \xrightarrow{\partial w_2} \frac{\partial y}{\partial w_2} \xrightarrow{\partial w_3}$ 

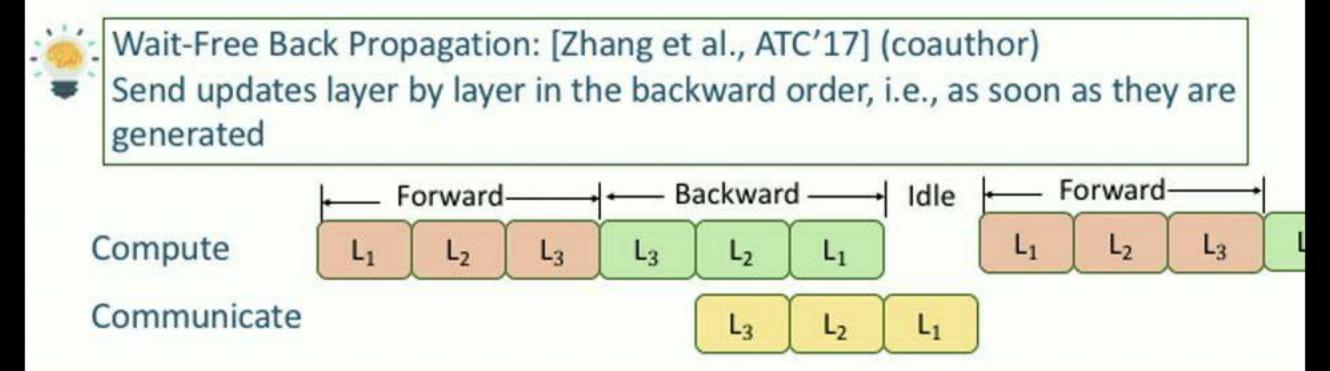
#### The Mini-Batch Computation of Deep Neural Networks



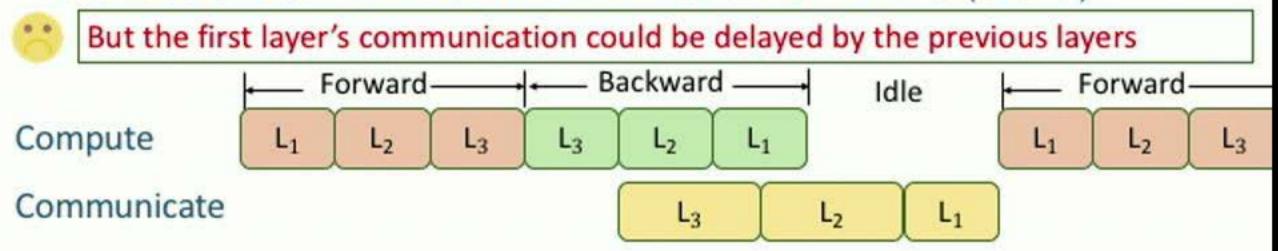
#### Opportunity:

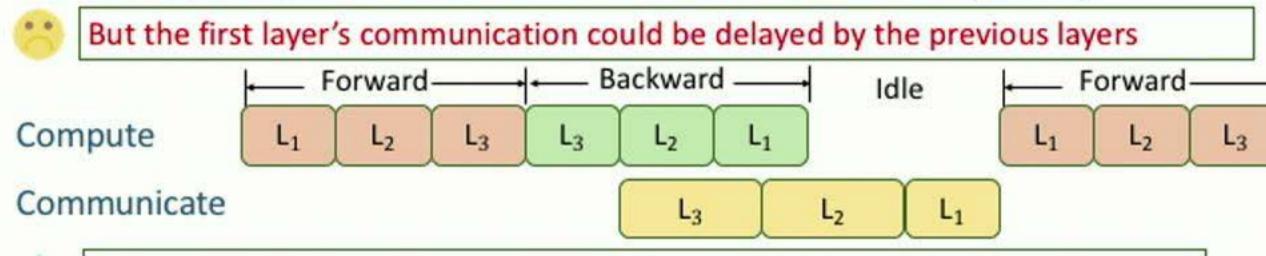
Not all parameters (updates) are needed (generated) at the same time

#### Schedule Communication Within A Mini-Batch for DNNs



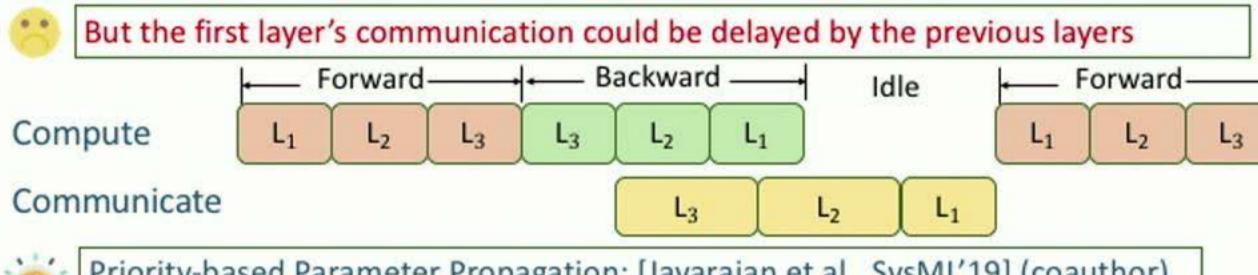
Overlap backward computation with communication within a mini-batch Ideally, computation is idle only during the first layer's communication





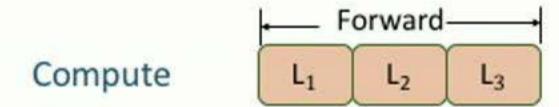


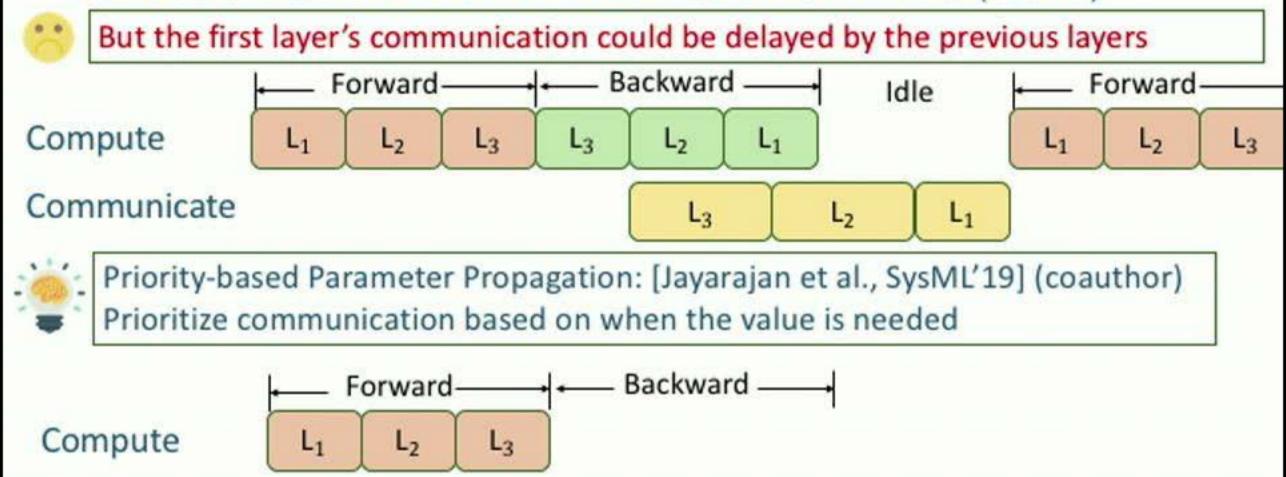
Priority-based Parameter Propagation: [Jayarajan et al., SysML'19] (coauthor)
Prioritize communication based on when the value is needed

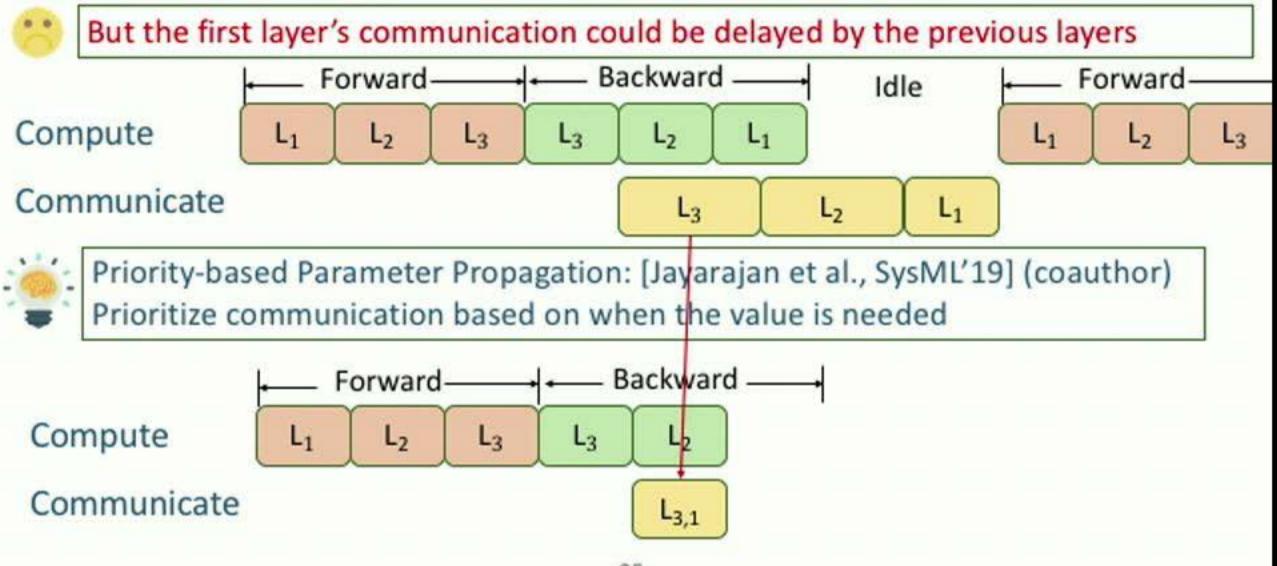


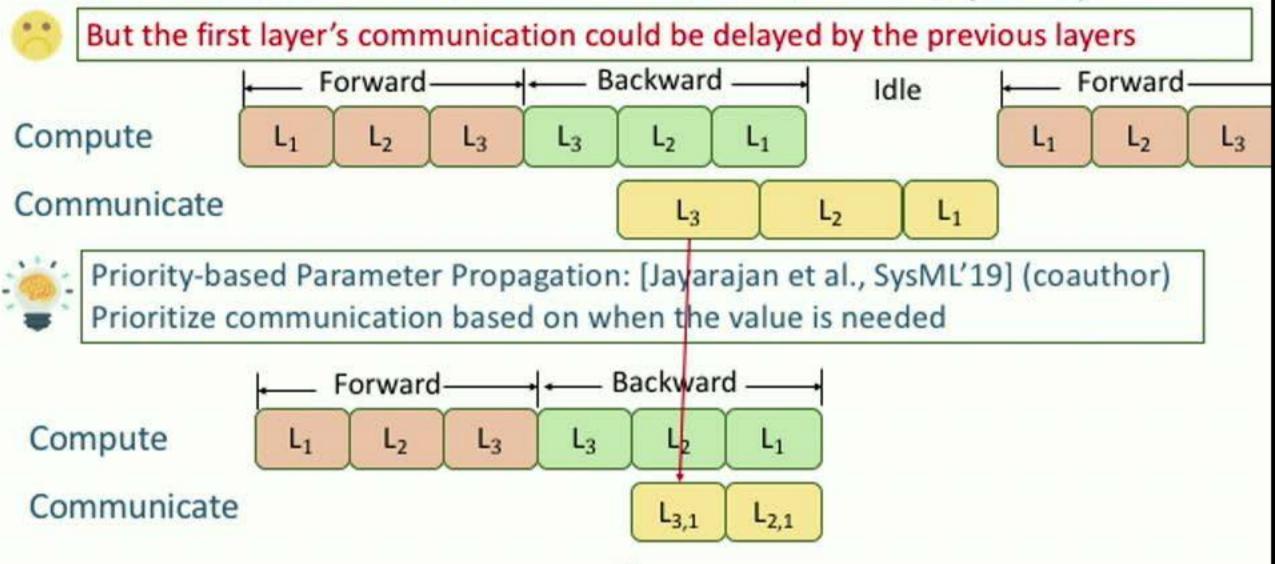


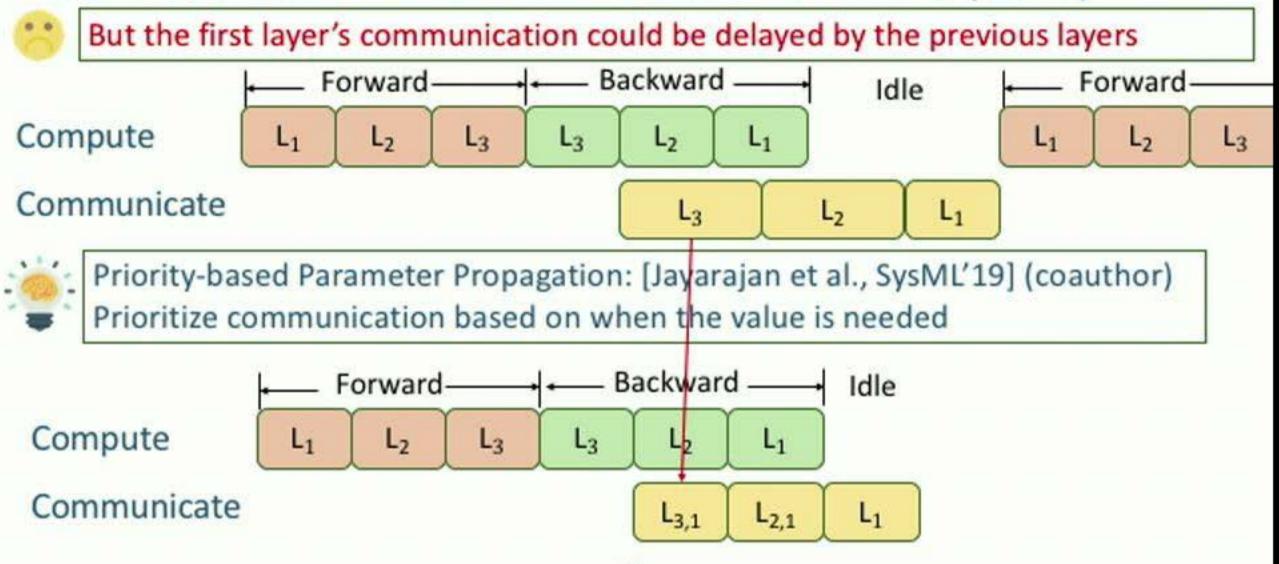
Priority-based Parameter Propagation: [Jayarajan et al., SysML'19] (coauthor)
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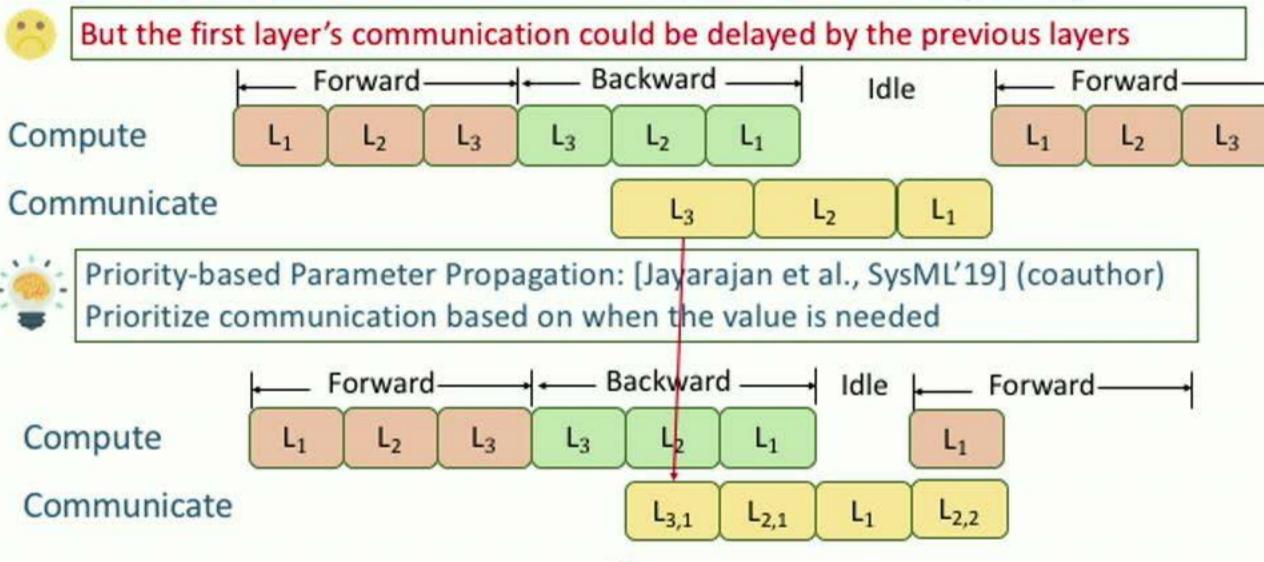


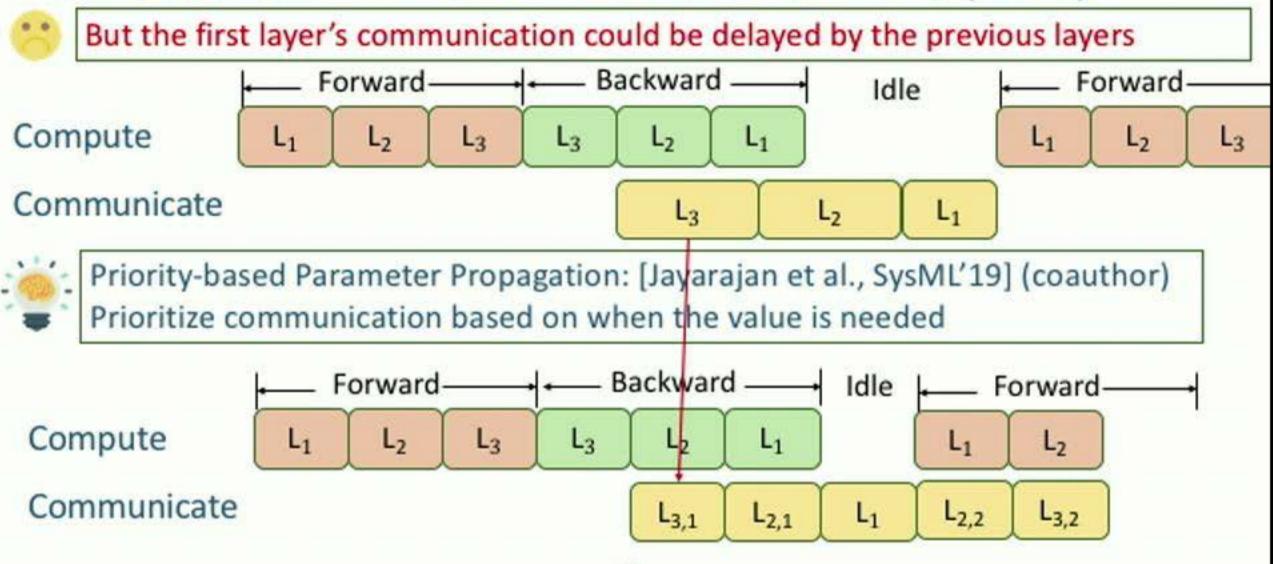


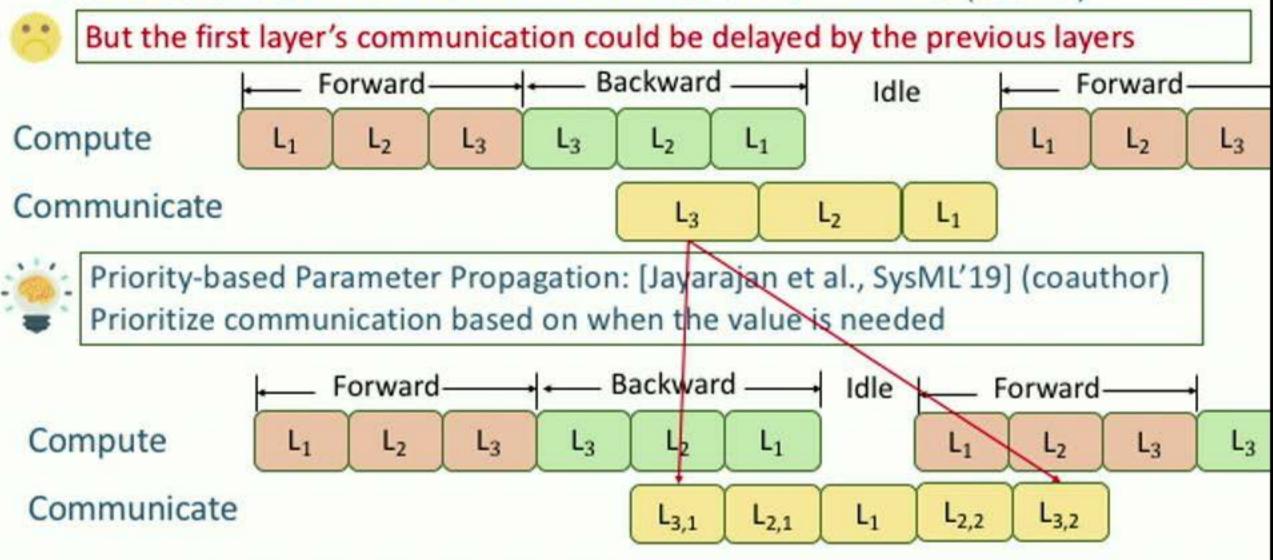




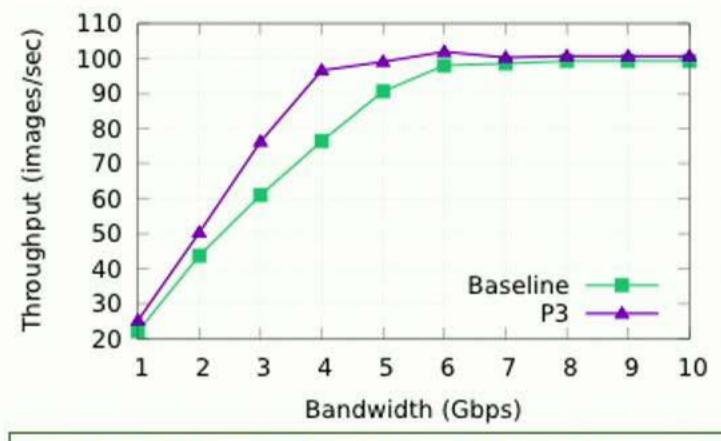






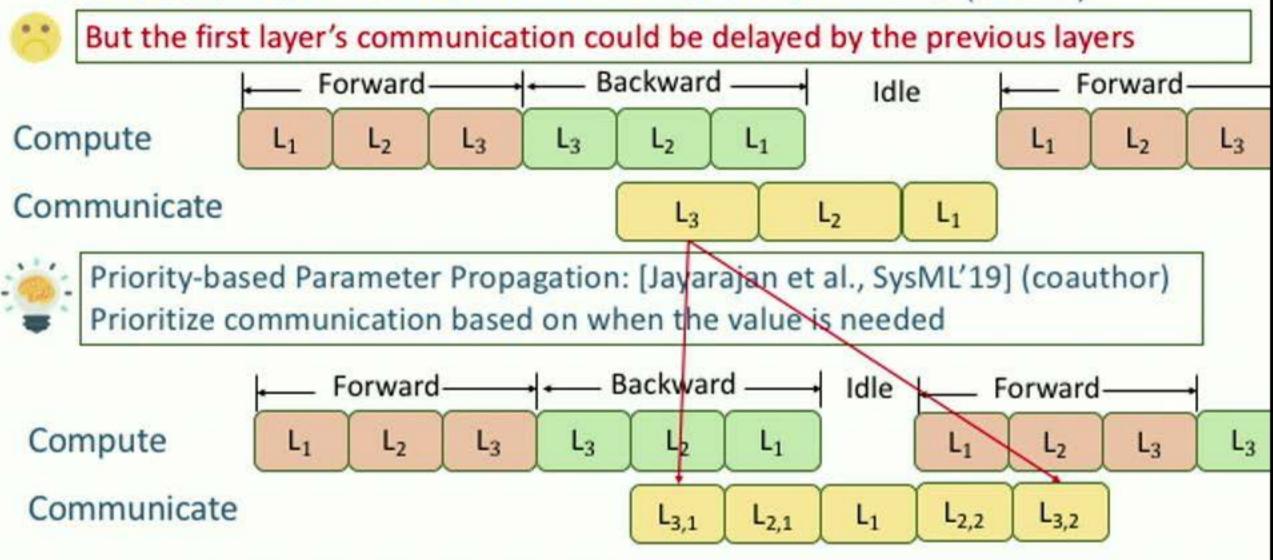


# P3 Experiment Results on MXNet

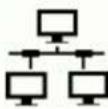


Baseline: MXNet (w/ Wait-Free Backpropagation)

Model: ResNet-50



# Scheduling within a Single Training Job

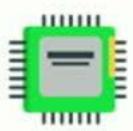


#### **Network Communication**

When and what to send?

Lead [SoCC'15, Best paper]

Coauthor [ATC'17] [SysML'19]



#### Computation

What to compute in parallel?

[EuroSys'19]



#### **Memory Allocation**

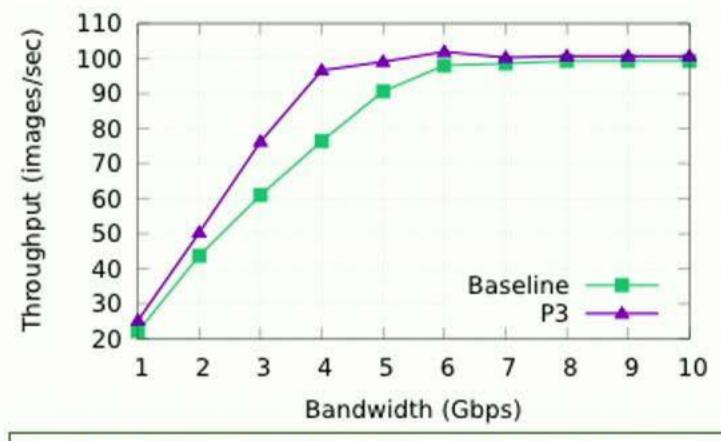
When and where to allocate?

[In preparation]

#### Highlights of results:

- Scheduling communication: up to 30% faster convergence
- Scheduling computation: even faster convergence with less programmer effort
- Scheduling memory: 10x bigger model on the same hardware

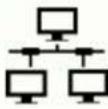
# P3 Experiment Results on MXNet



Baseline: MXNet (w/ Wait-Free Backpropagation)

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# Scheduling within a Single Training Job

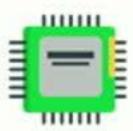


#### **Network Communication**

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#### Computation

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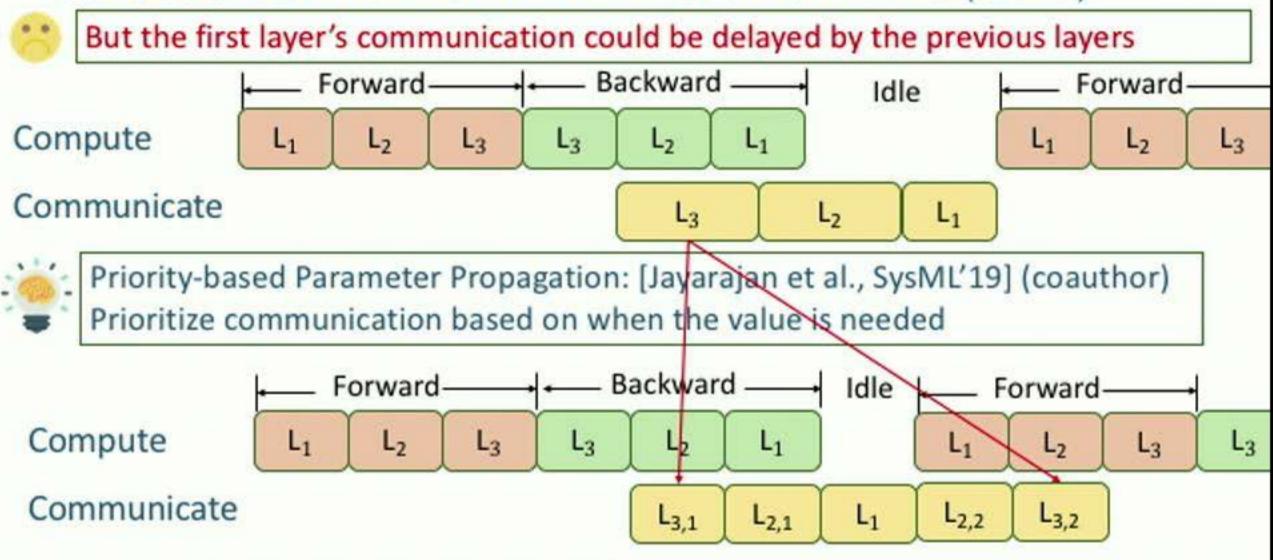
#### **Memory Allocation**

When and where to allocate?

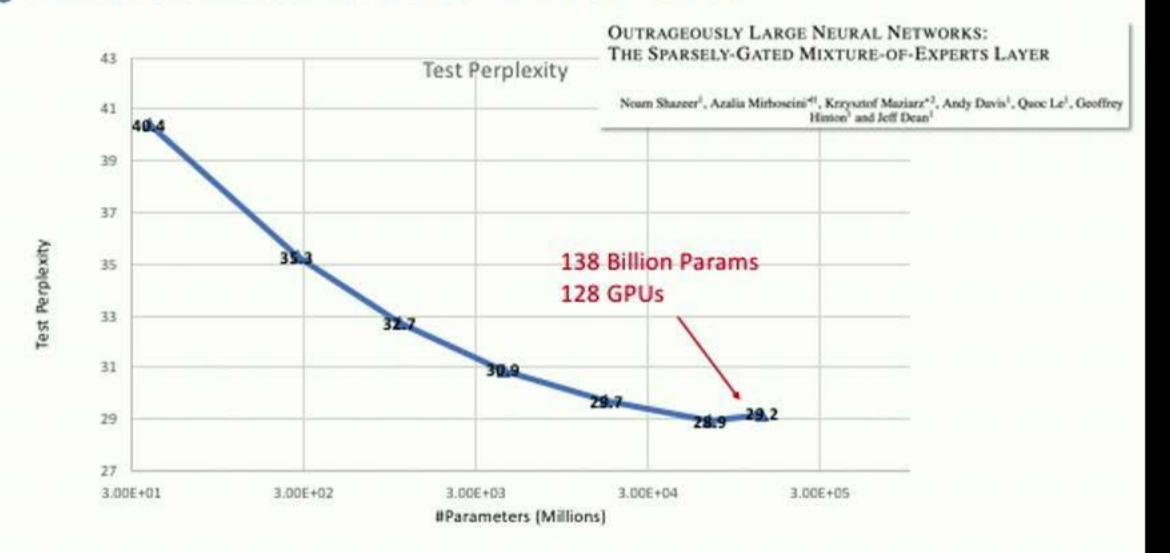
[In preparation]

#### Highlights of results:

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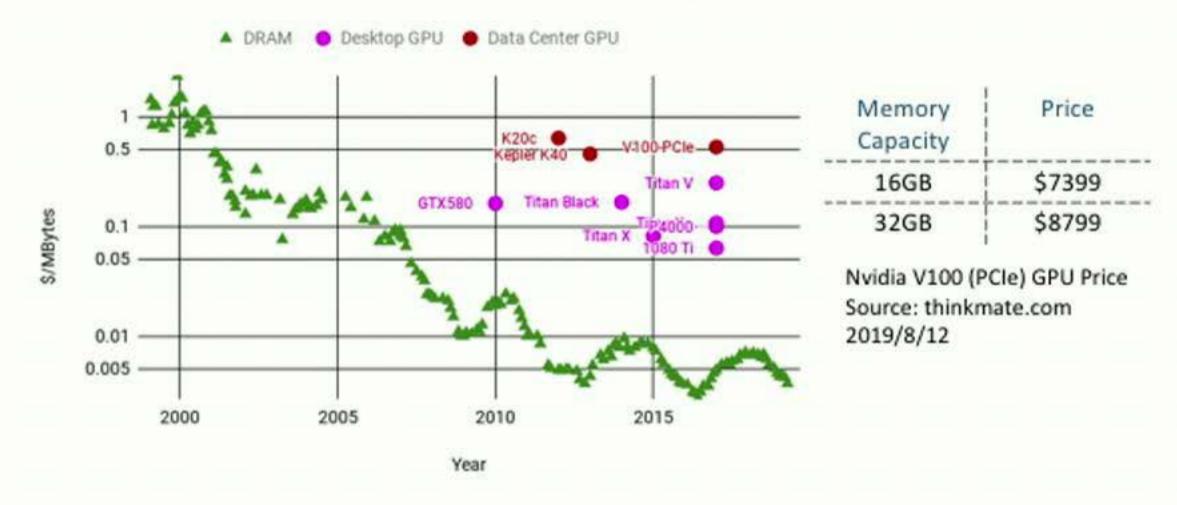
# Larger Models Lead To Better Performance



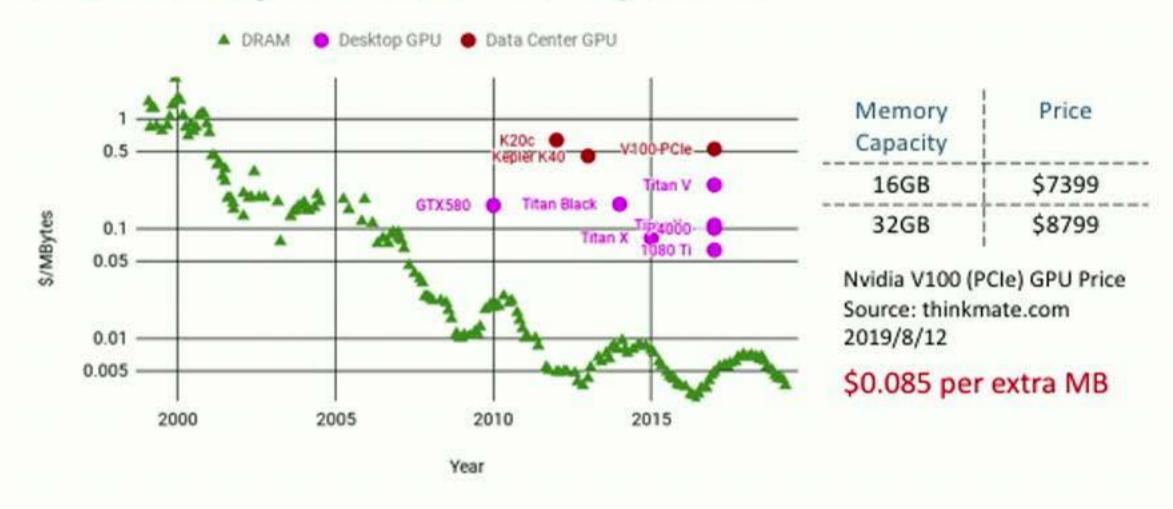
# GPU Memory Is Limited And Expensive



#### GPU Memory Is Limited And Expensive



#### GPU Memory Is Limited And Expensive



### Many Previous Works on Improving Memory Efficiency

#### Gradient checkpointing (leveraging recomputation)

Training Deep Nets with Sublinear Memory Cost [Chen et al., arXiv'16]

Memory-Efficient Backpropagation Through Time [Gruslys et al., arXiv'16]

...

#### Memory swapping (leveraging cheaper host memory)

Dynamic Control Flow in Large-Scale Machine Learning [Yu, EuroSys'19]

vDNN: virtualized deep neural networks for scalable, memory-efficient neural network design [Rhu et al., MICRO'16]

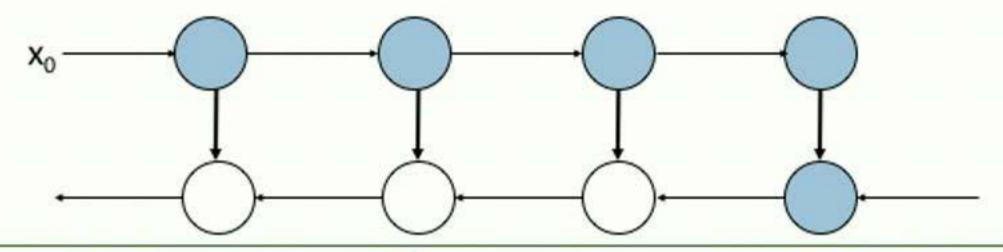
Training Deeper Models by GPU Memory Optimization on TensorFlow [Meng et al., MLSys'17]

Superneurons: dynamic GPU memory management for training deep neural networks [Wang et al., PPoPP'18]

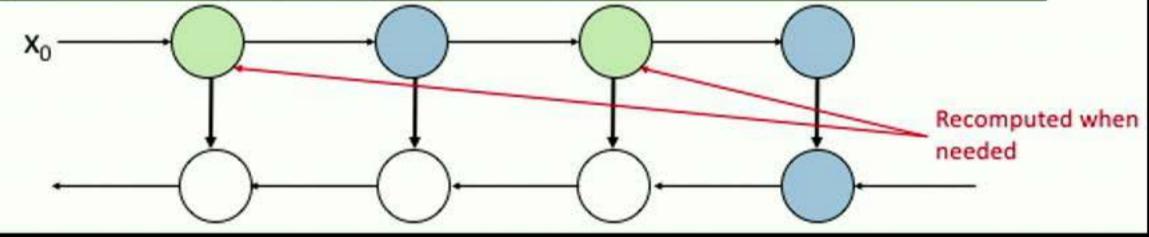
TensorFlow Grapper memory optimizer

# Background: Gradient Checkpointing

Original computation graph for backpropagation, O(M) memory cost

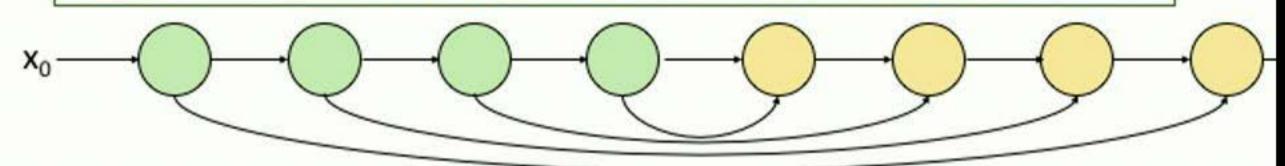


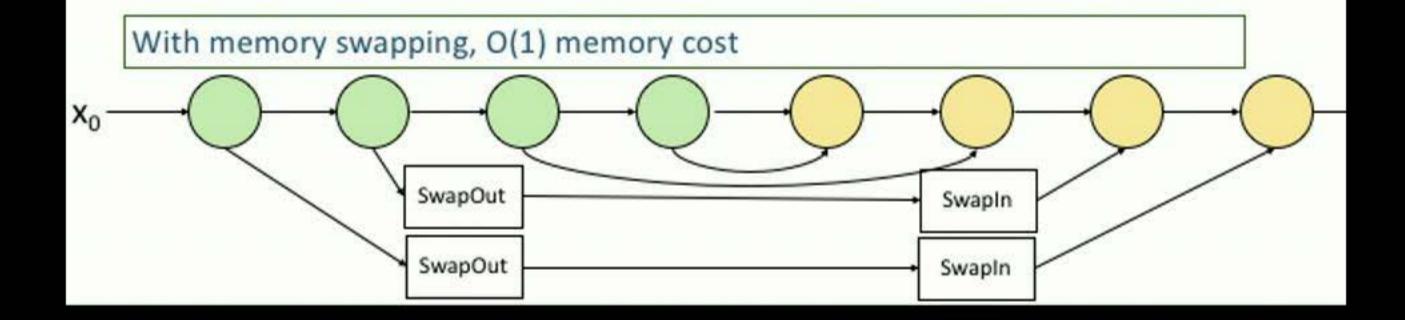
With gradient checkpointing,  $O(\sqrt{N})$  memory cost



### Background: Memory Swapping

Original computation graph for backpropagation, O(M) memory cost





#### They Work Well for Linear Graphs

Most nodes are "graph separator nodes": removing each one separates the graph into two disjoint subgraphs

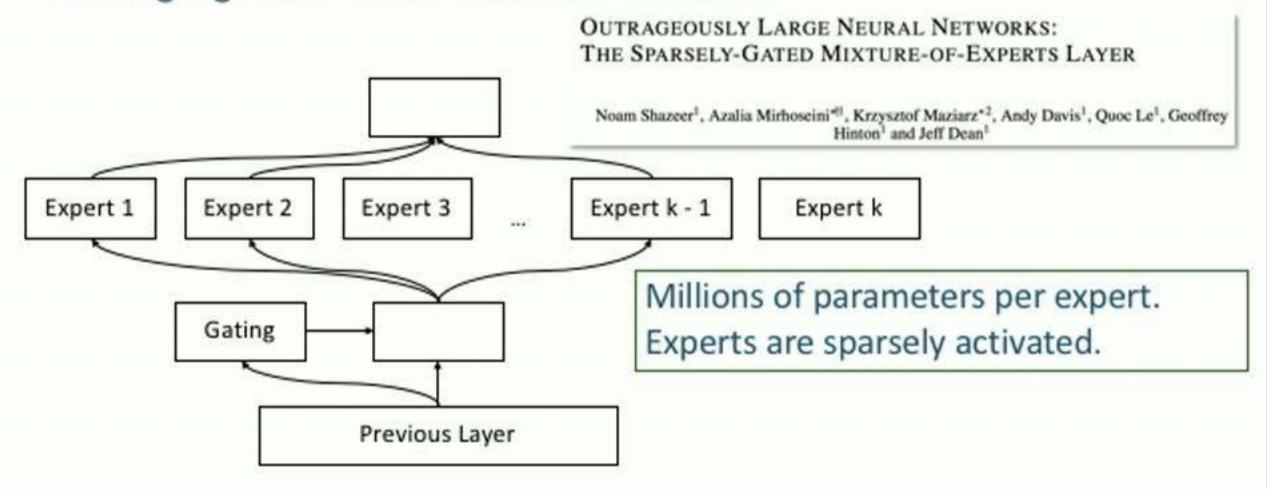
Gradient checkpointing: easy to determine which nodes to checkpoint.

Limited freedom regarding scheduling

Memory swapping: easy to determine what and when to swap

Problem: many neural network graphs are not linear! Some layers have an excessive amount of parallelism.

#### **Emerging Non-linear Neural Networks**



#### Goal: General Memory-Efficient DL On TensorFlow



Linear and nonlinear computation graphs

Implement and evaluate on TensorFlow

Transparent to applications.

#### **Existing memory optimizations for TensorFlow:**

Gradient checkpointing (Bolatov et al., GitHub'17]):

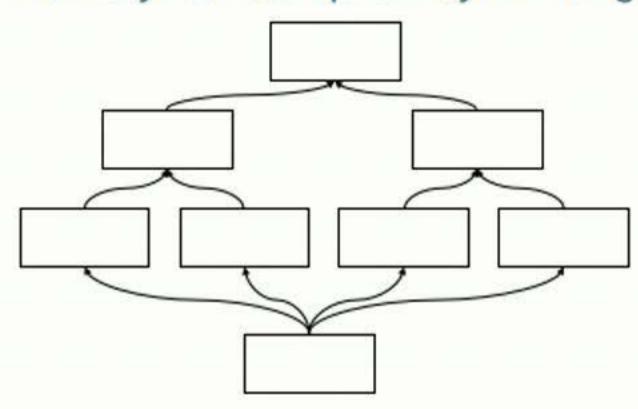
Limited to linear graphs; requires non-trivial changes to application program

Grappler memory swapping pass:

Limited to linear graphs

WhileLoop memory swapping ([Yuan et al., EuroSys'18]):

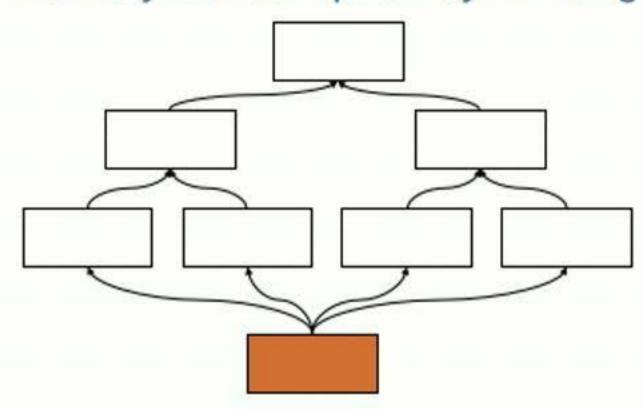
Operation specific memory reduction



TensorFlow

Breath-first traversal

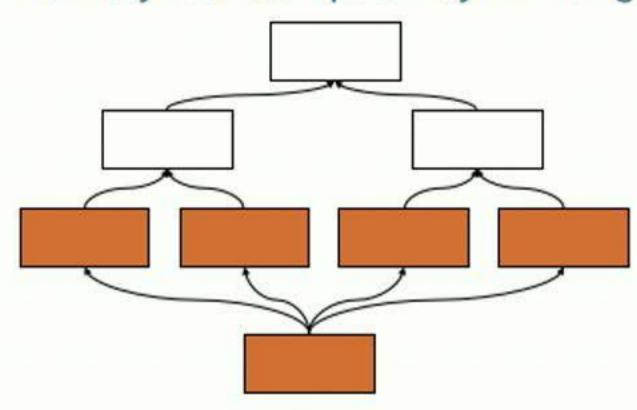
Max. parallelism



TensorFlow

Breath-first traversal

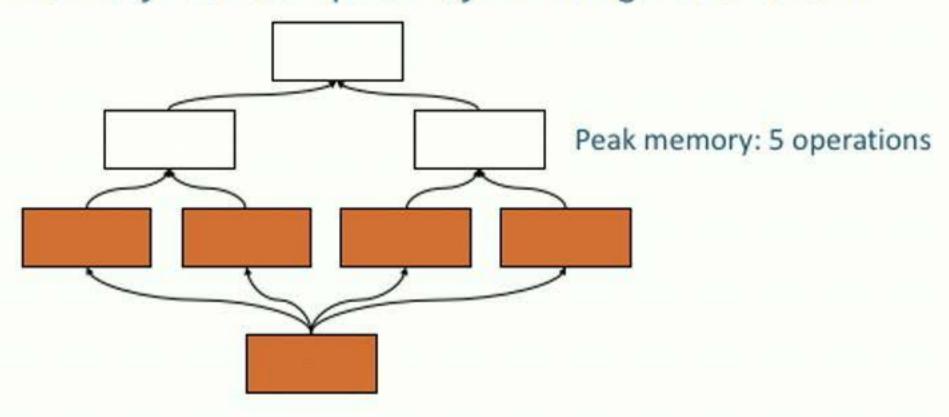
Max. parallelism



TensorFlow

Breath-first traversal

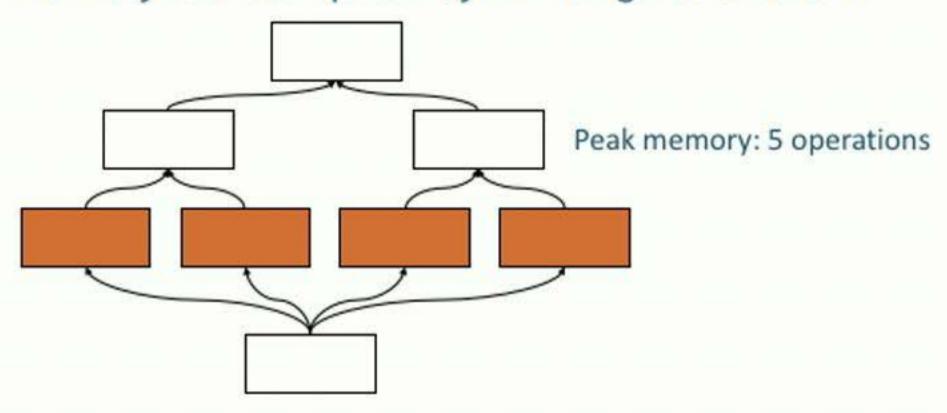
Max. parallelism



TensorFlow

Breath-first traversal

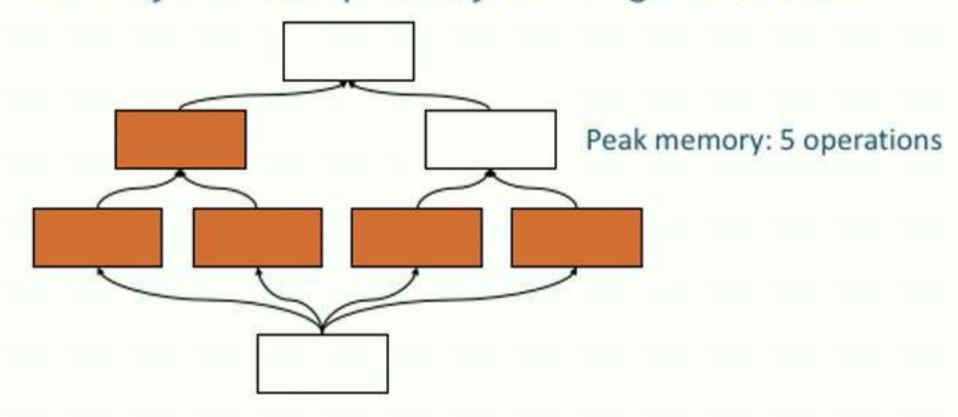
Max. parallelism



TensorFlow

Breath-first traversal

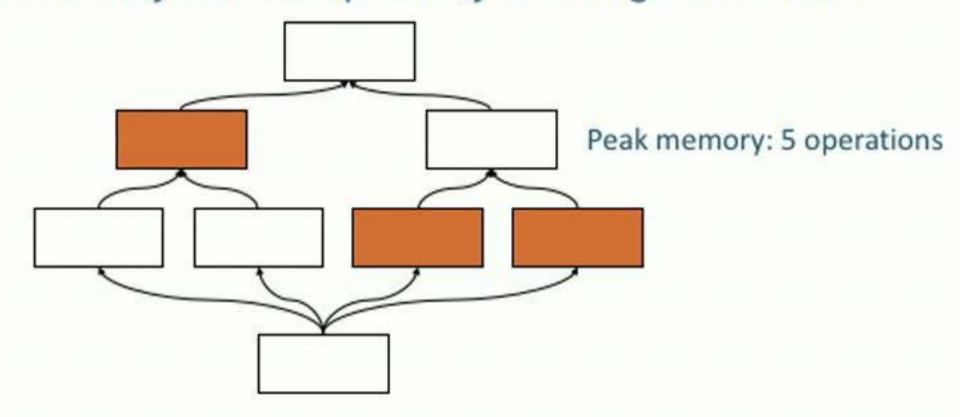
Max. parallelism



TensorFlow

Breath-first traversal

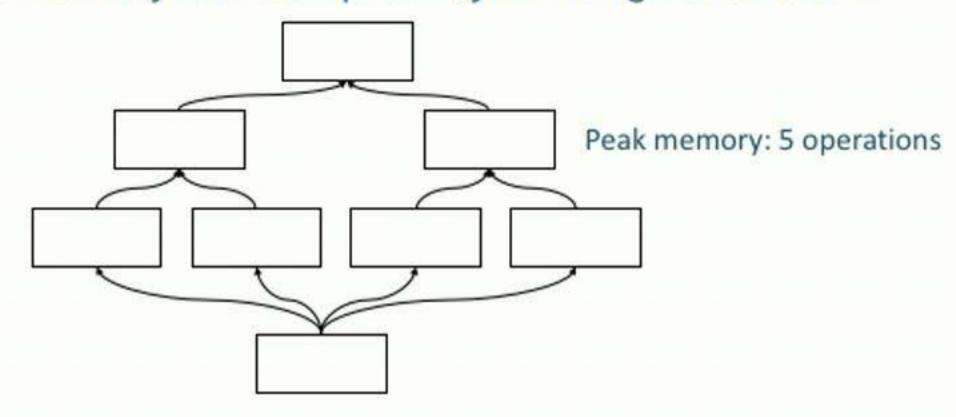
Max. parallelism



TensorFlow

Breath-first traversal

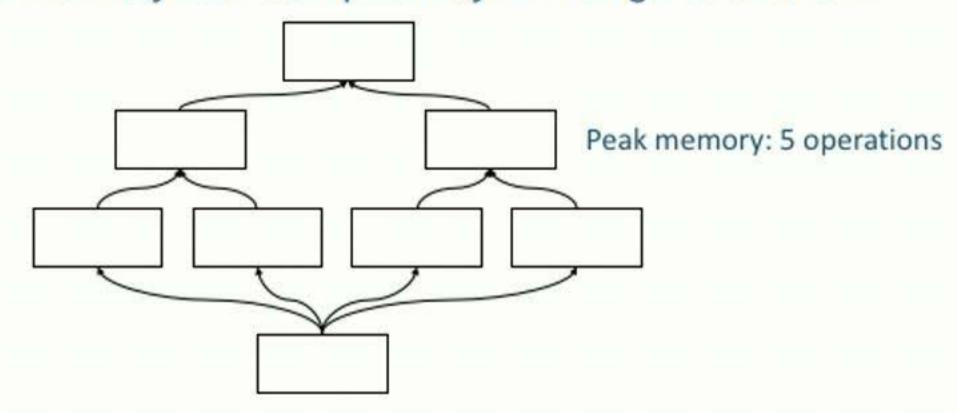
Max. parallelism



TensorFlow

Breath-first traversal

Max. parallelism



TensorFlow

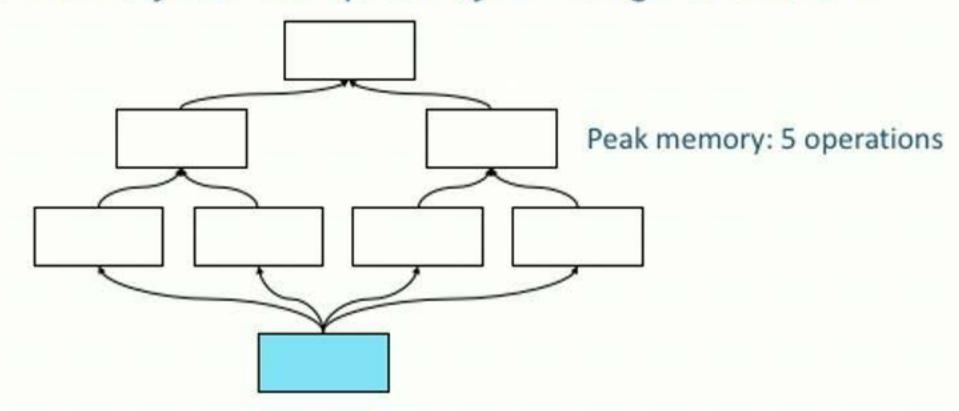
Breath-first traversal

Max. parallelism

Max. memory

Linearize the graph

No parallelism Min. memory



TensorFlow

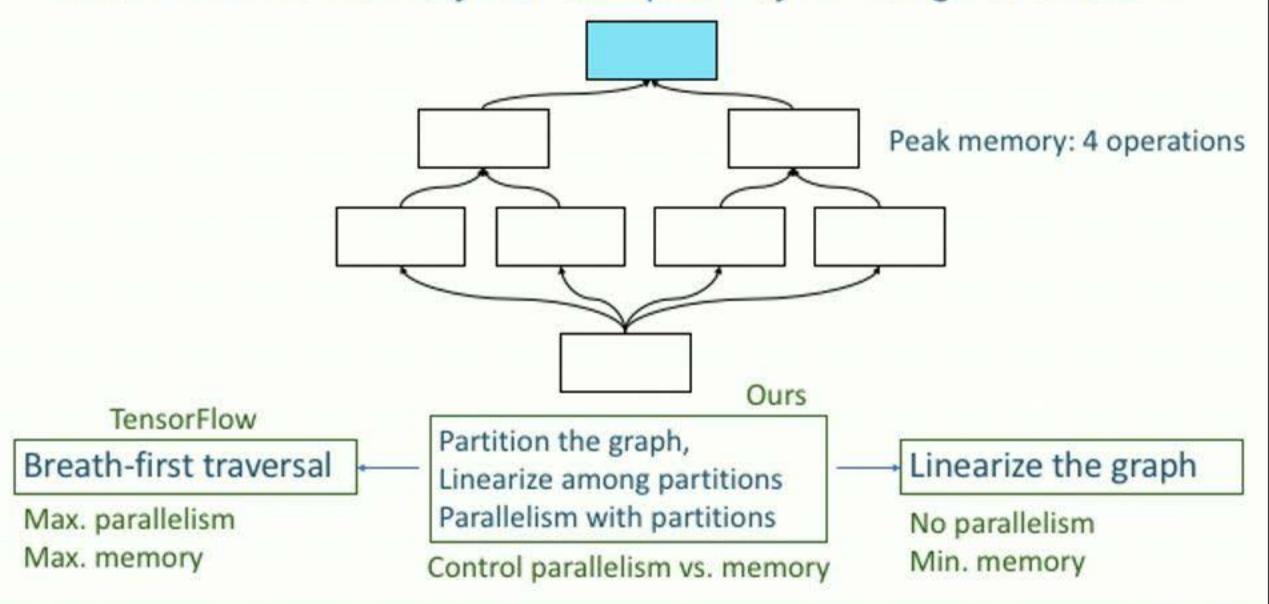
Breath-first traversal

Max. parallelism

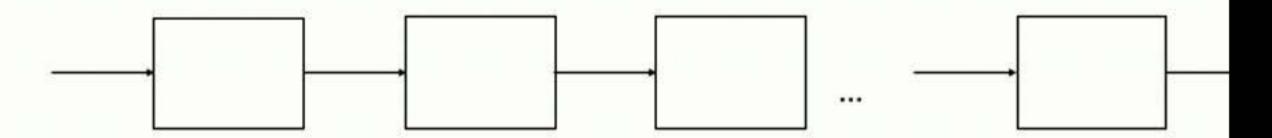
Max. memory

Linearize the graph

No parallelism Min. memory



#### Idea #2: Offload GPU Tensors To Host Memory

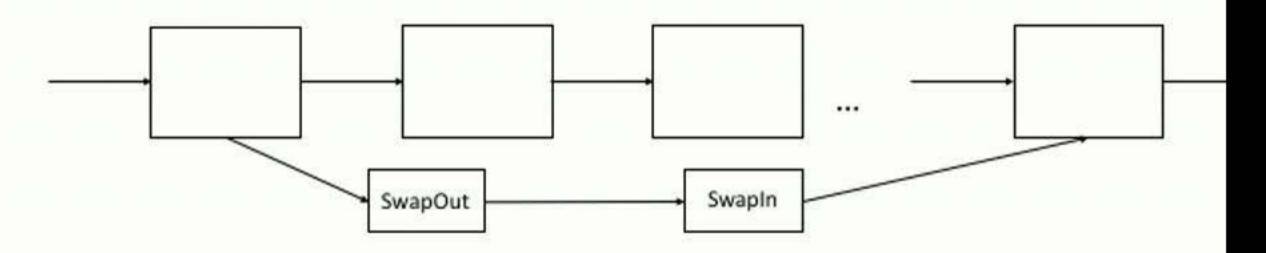


Transformer
Use MoE as the Feed Forward layer
12 MoEs
32 experts per MoE
2M params per expert
~800M parameters total

Peak memory:

9.5GB to 6.8GB

#### Idea #2: Offload GPU Tensors To Host Memory



Transformer

Use MoE as the Feed Forward layer

12 MoEs

32 experts per MoE

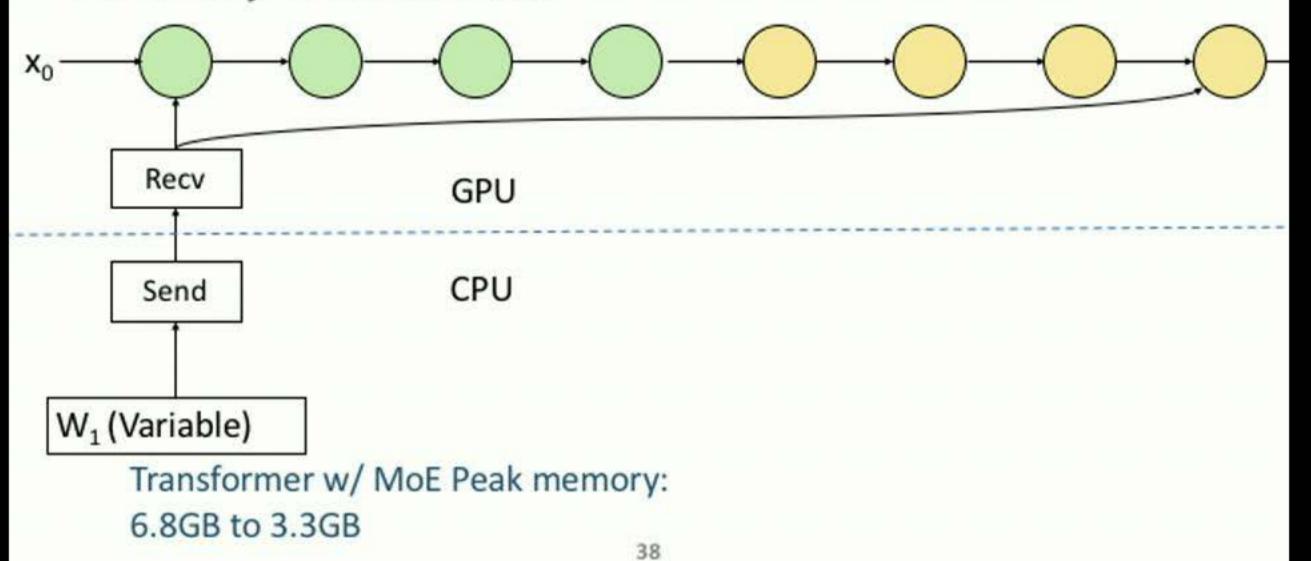
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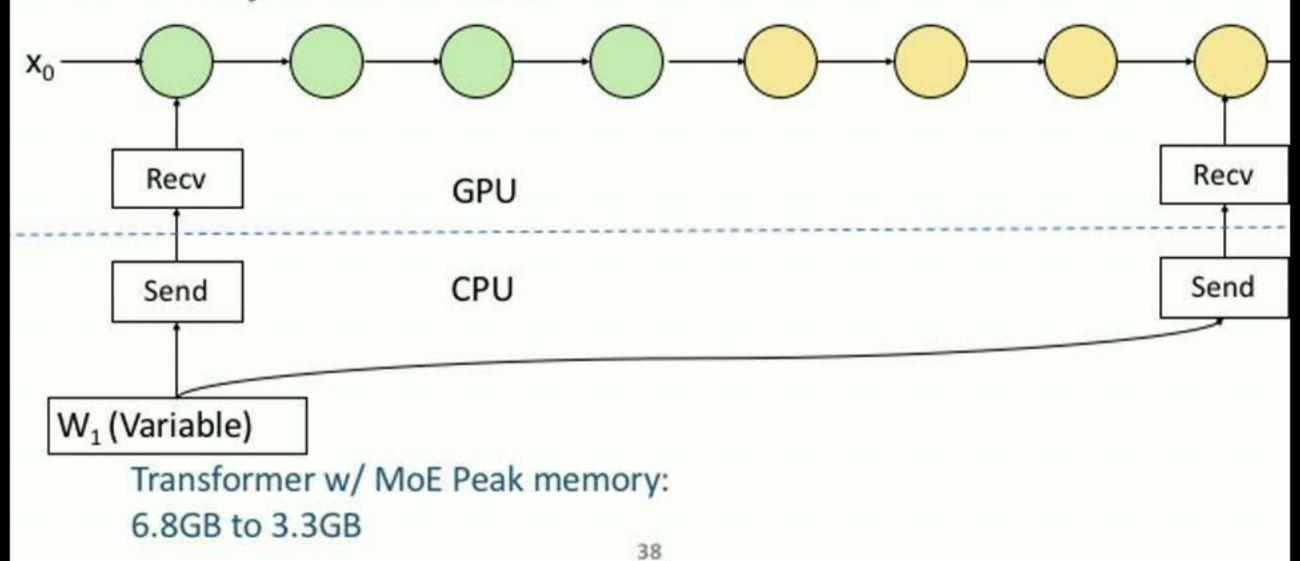
Peak memory:

9.5GB to 6.8GB

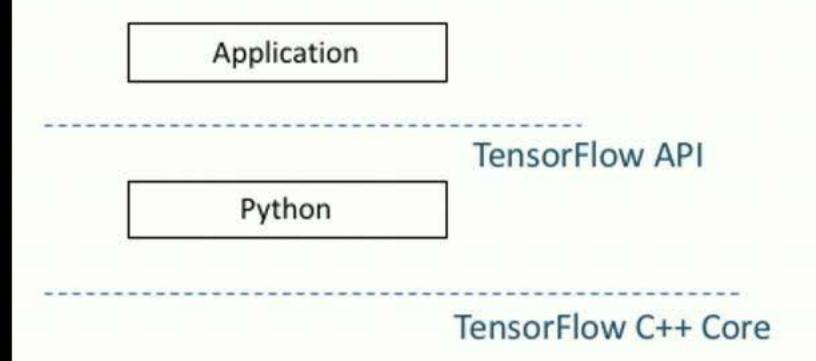
# Idea #3: Place Persistent Tensors on Host Memory & Send To GPU Only When Needed



# Idea #3: Place Persistent Tensors on Host Memory & Send To GPU Only When Needed



#### Implementation & Experiment Setup



Experiment platform:
32 vCPU cores
64GB memory
1 GPU per machine
Nvidia TitanX Maxwell
12GB GPU Memory

**Grappler Optimizers** 

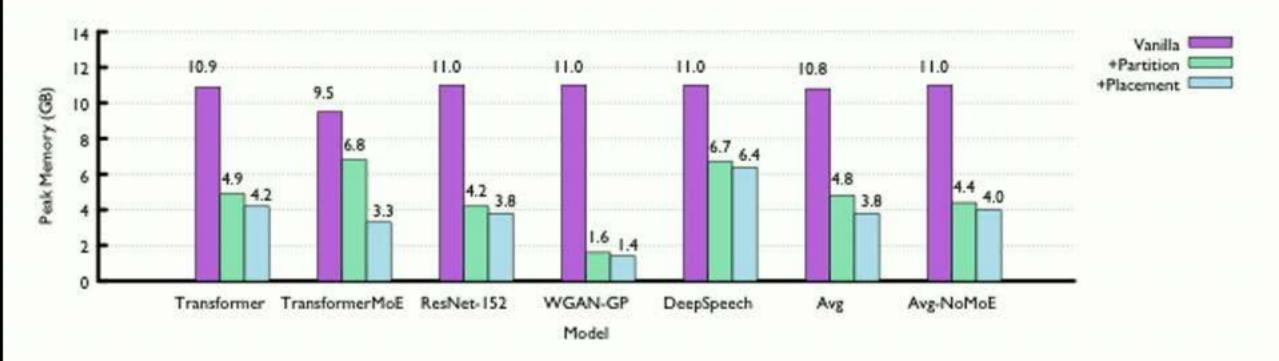
Executor

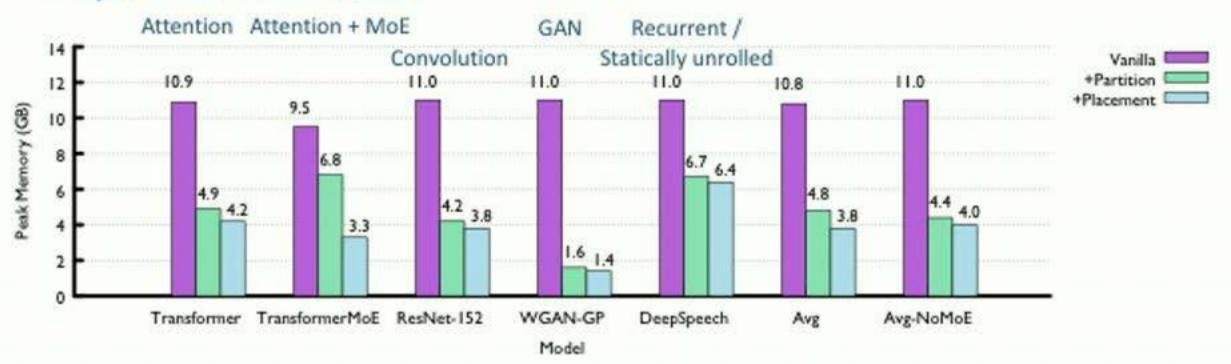
GraphPartition

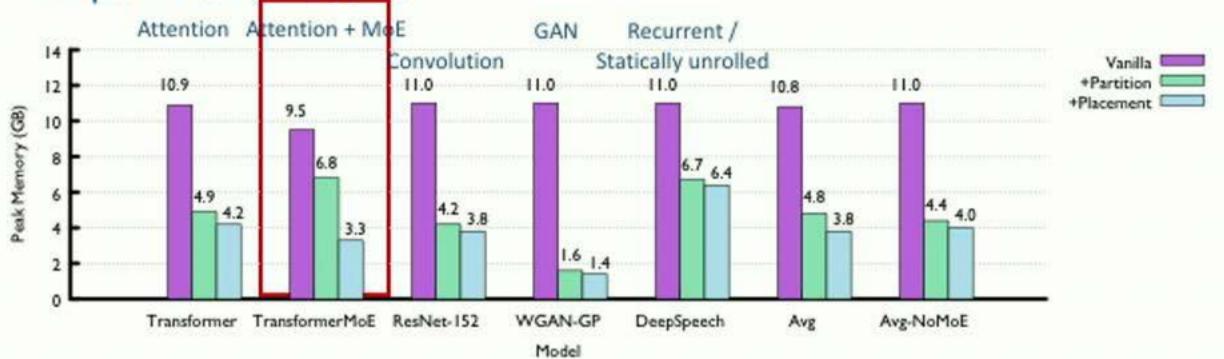
Graph Partition & Memory Swapping

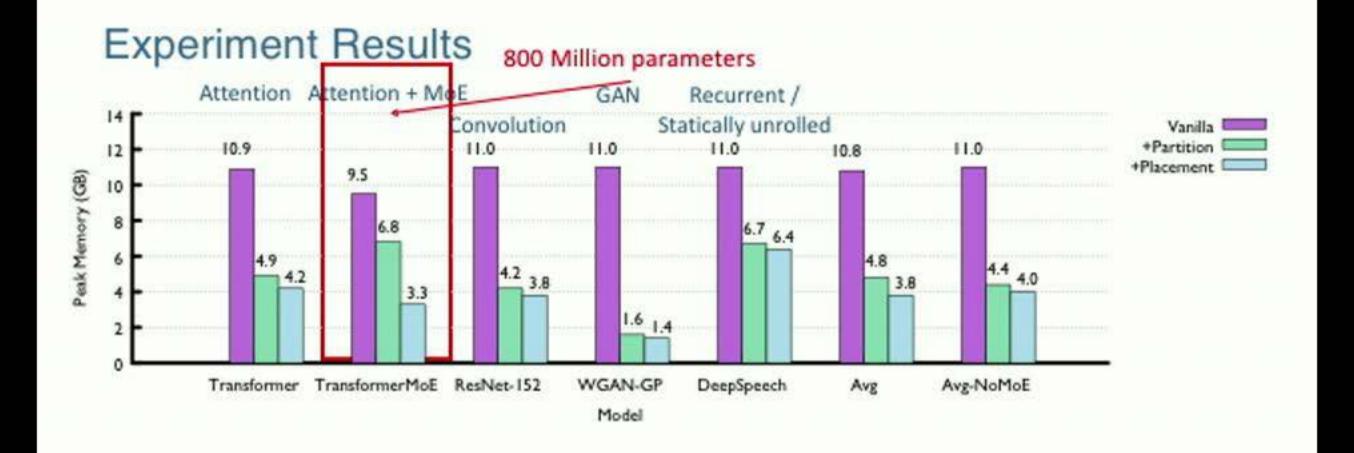
Scheduling

Send, Recv nodes

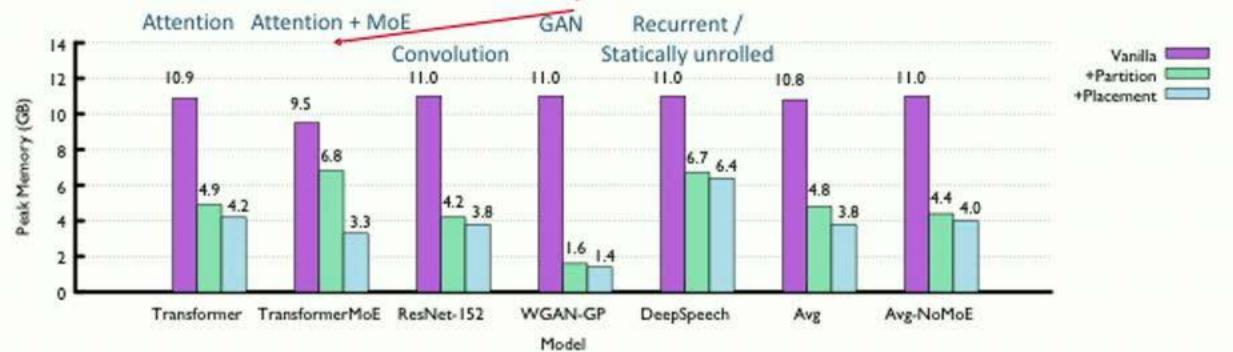


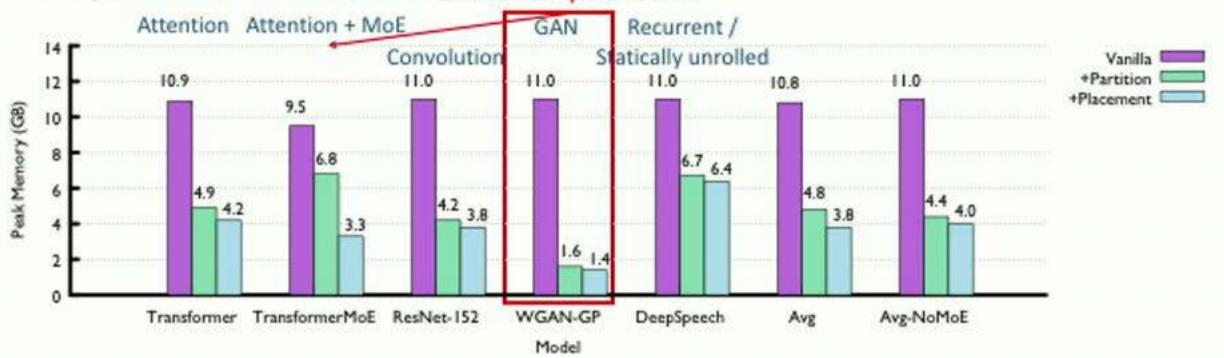


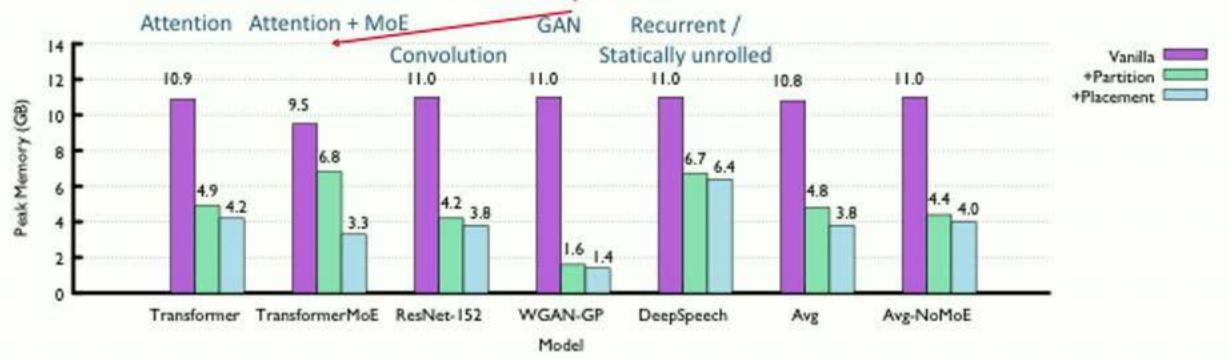


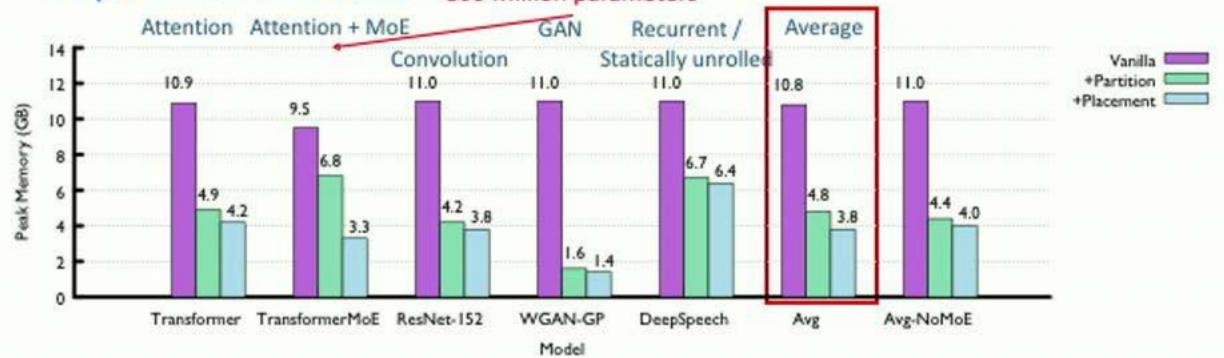




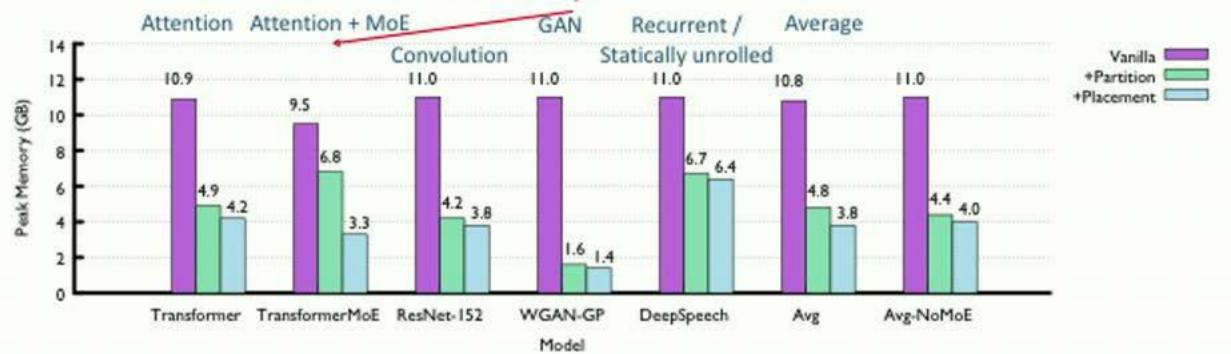


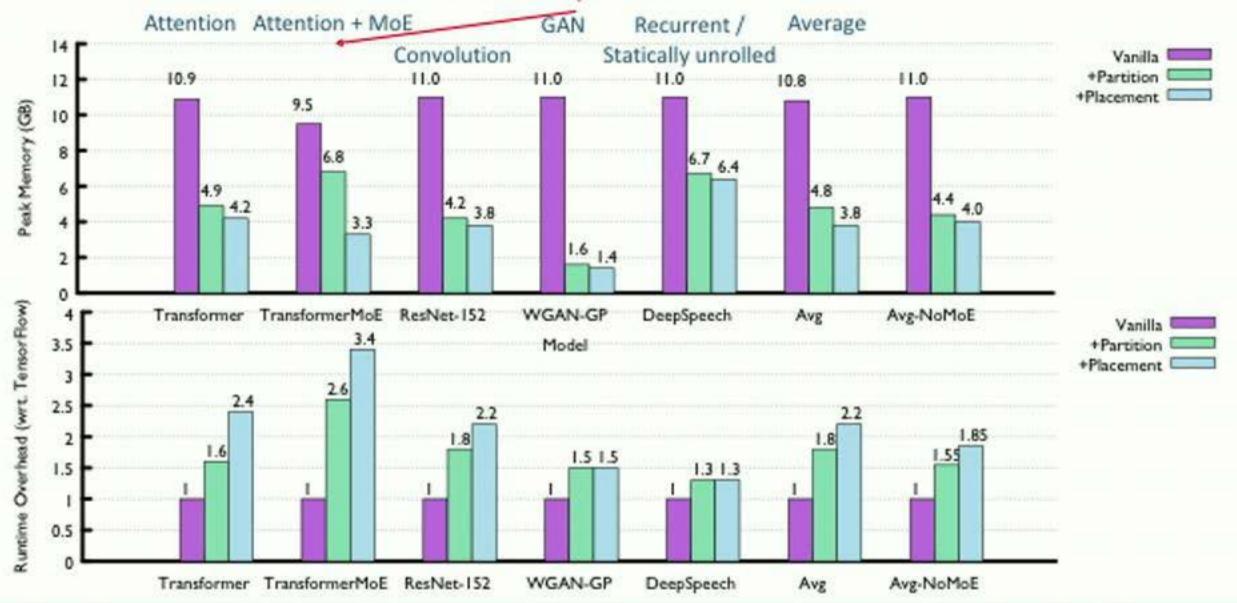












**Experiment Results** 800 Million parameters Attention Attention + MoE GAN Average Recurrent / Convolution Statically unrolled Vanilla -+Partition 10.9 11.0 11.0 11.0 11.0 10.8 +Placement 9.5 Peak Memory (GB) 6.7 6.4 4.2 3.8 3.3 1.6 1.4 Runtime Overhead (wrt. TensorRow) ransformer MoE ResNet-152 Avg-NoMoE Transformer WGAN-GP DeepSpeech Avg Vanilla 1 3.5 Model +Partition +Placement = 2.4 1.85 1.5 1.5 1.3 1.3 1.5

WGAN-GP

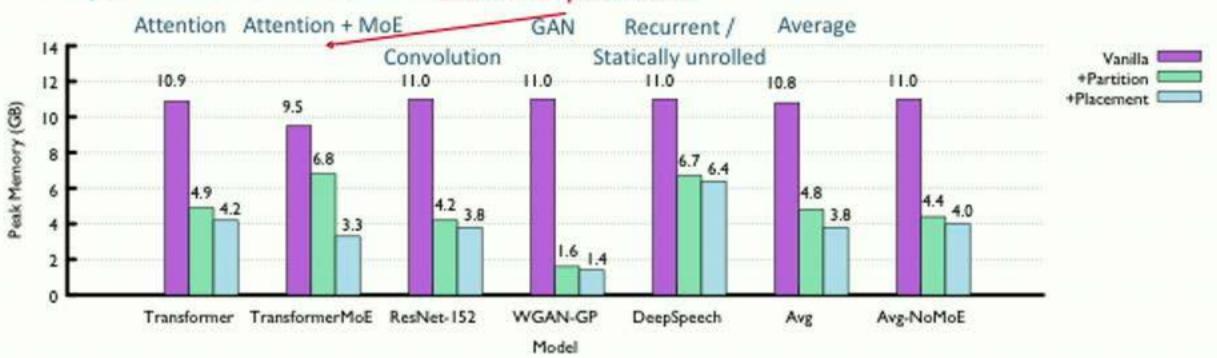
DeepSpeech

Avg-NoMoE

ransformerMoE

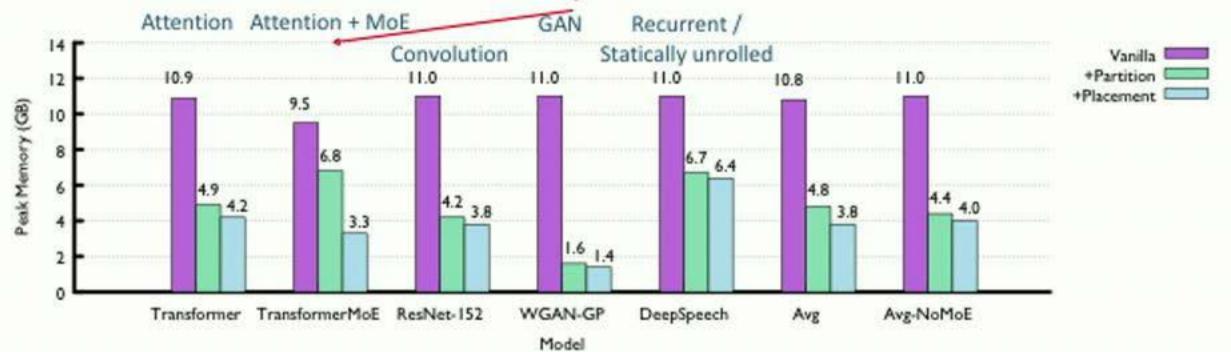
ResNet-152

Transformer

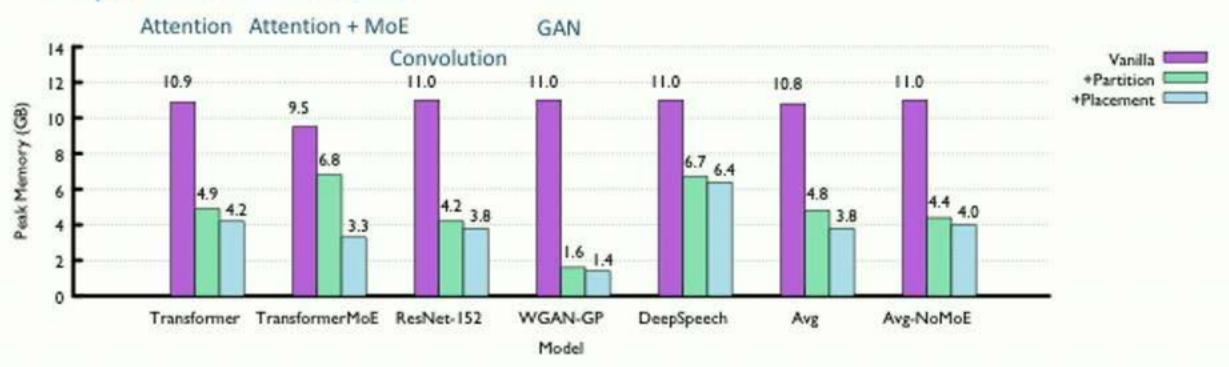


# Experiment Results 800 N

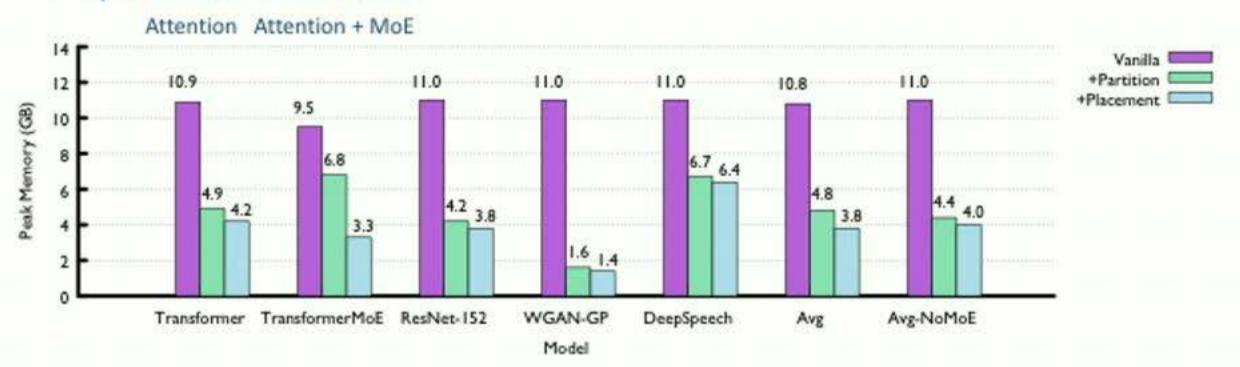




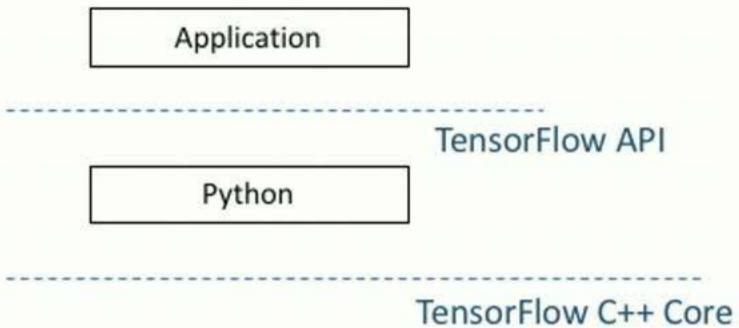
# **Experiment Results**



# **Experiment Results**



### Implementation & Experiment Setup



W C++ Core 12GB GPU Memory

GraphPartition

Experiment platform:

1 GPU per machine

32 vCPU cores

64GB memory

**Grappler Optimizers** 

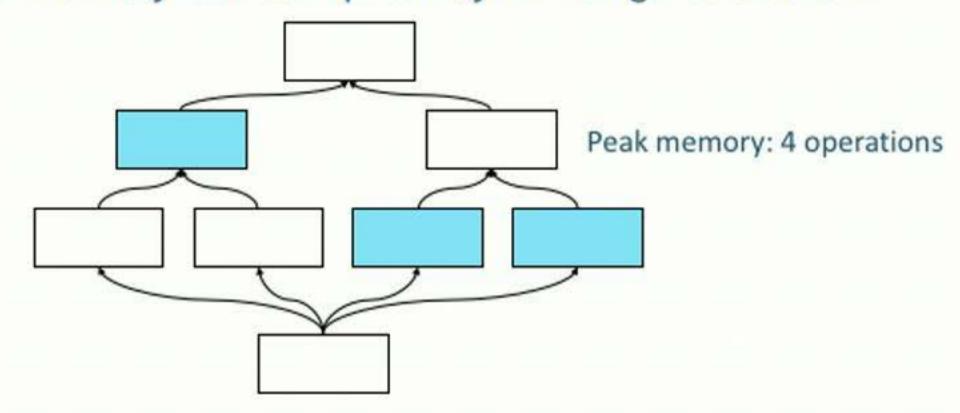
Graph Partition & Memory Swapping

Executor

Scheduling

Send, Recv nodes

### Idea #1: Limit Memory Consumption by Limiting Parallelism



TensorFlow

Breath-first traversal

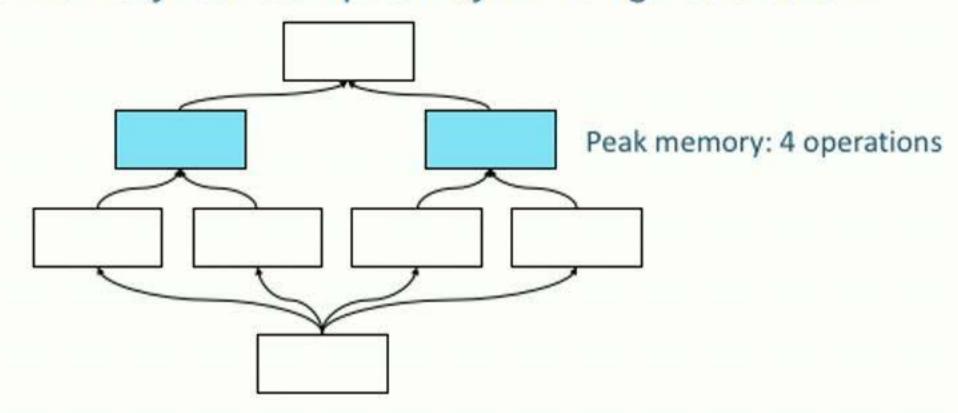
Max. parallelism

Max. memory

Linearize the graph

No parallelism Min. memory

### Idea #1: Limit Memory Consumption by Limiting Parallelism



TensorFlow

Breath-first traversal

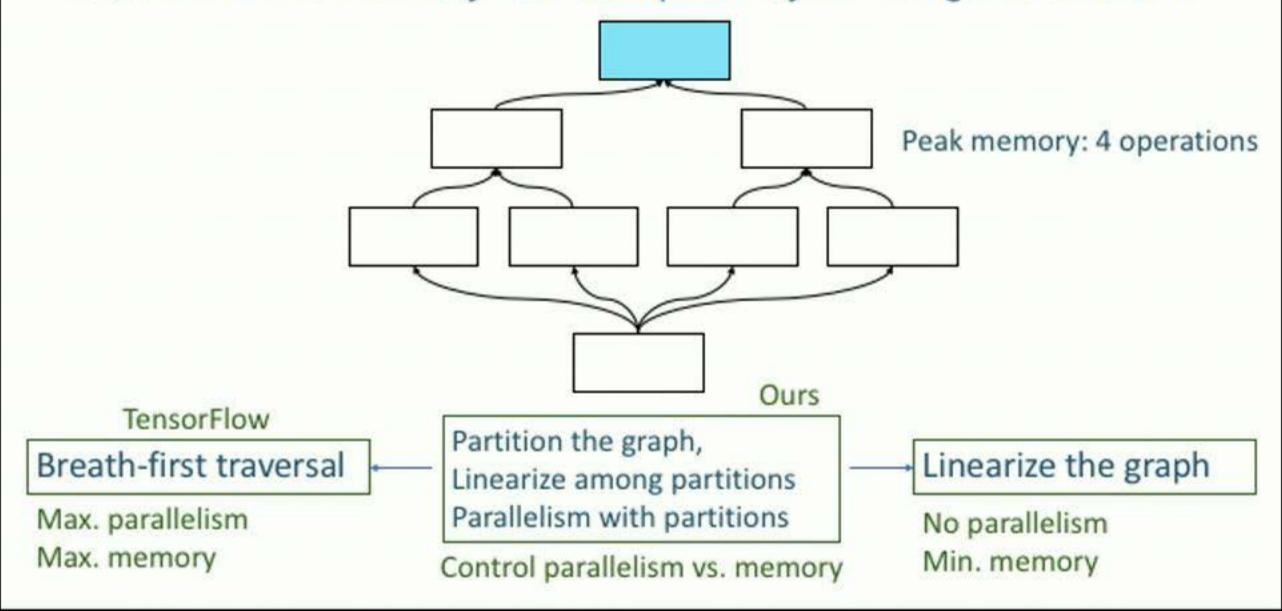
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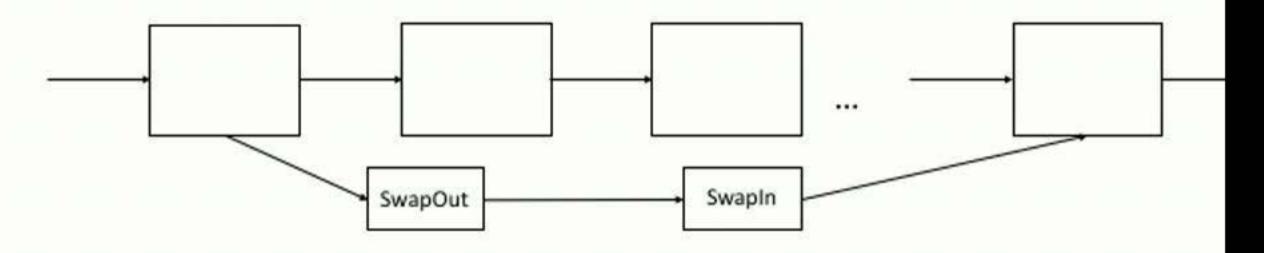
Linearize the graph

No parallelism Min. memory

## Idea #1: Limit Memory Consumption by Limiting Parallelism



# Idea #2: Offload GPU Tensors To Host Memory



Transformer

Use MoE as the Feed Forward layer

12 MoEs

32 experts per MoE

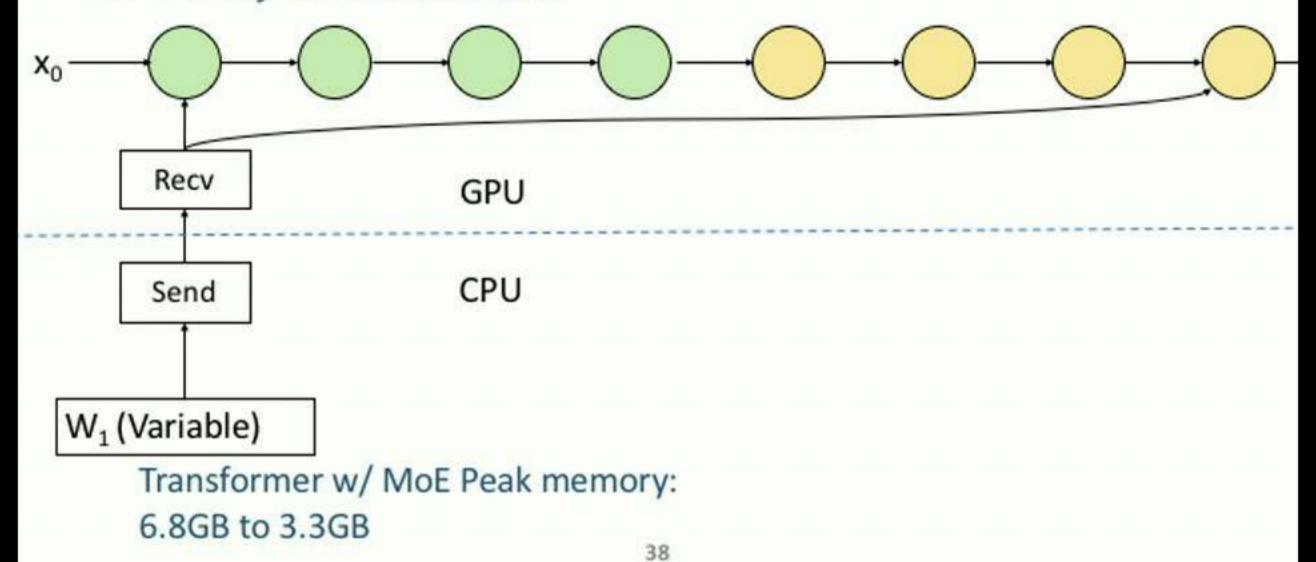
2M params per expert

~800M parameters total

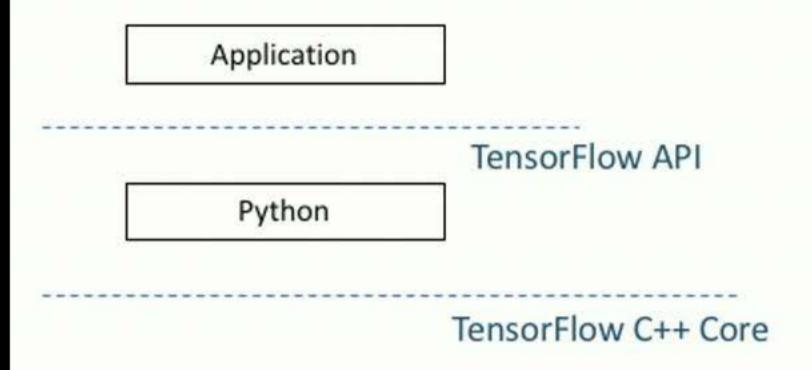
Peak memory:

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# Idea #3: Place Persistent Tensors on Host Memory & Send To GPU Only When Needed



### Implementation & Experiment Setup



Experiment platform:
32 vCPU cores
64GB memory
1 GPU per machine
Nvidia TitanX Maxwell
12GB GPU Memory

**Grappler Optimizers** 

Executor

GraphPartition

Graph Partition & Memory Swapping

Scheduling

Send, Recv nodes

**Experiment Results** 800 Million parameters Attention Attention + MoE GAN Average Recurrent / Convolution Statically unrolled Vanilla -\*Partition 10.9 11.0 11.0 11.0 11.0 10.8 +Placement 9.5 Peak Memory (GB) 6.7 6.4 4.4 4.0 4.2 3.8 3.3 1.6 1.4 Runtime Overhead (wrt. TensorRow) ransformerMoE ResNet-152 Avg-NoMoE Transformer WGAN-GP DeepSpeech Avg Vanilla 1 3.5 Model +Partition +Placement 2.4 1.85 1.5 1.5 1.3 1.3 1.5

WGAN-GP

DeepSpeech

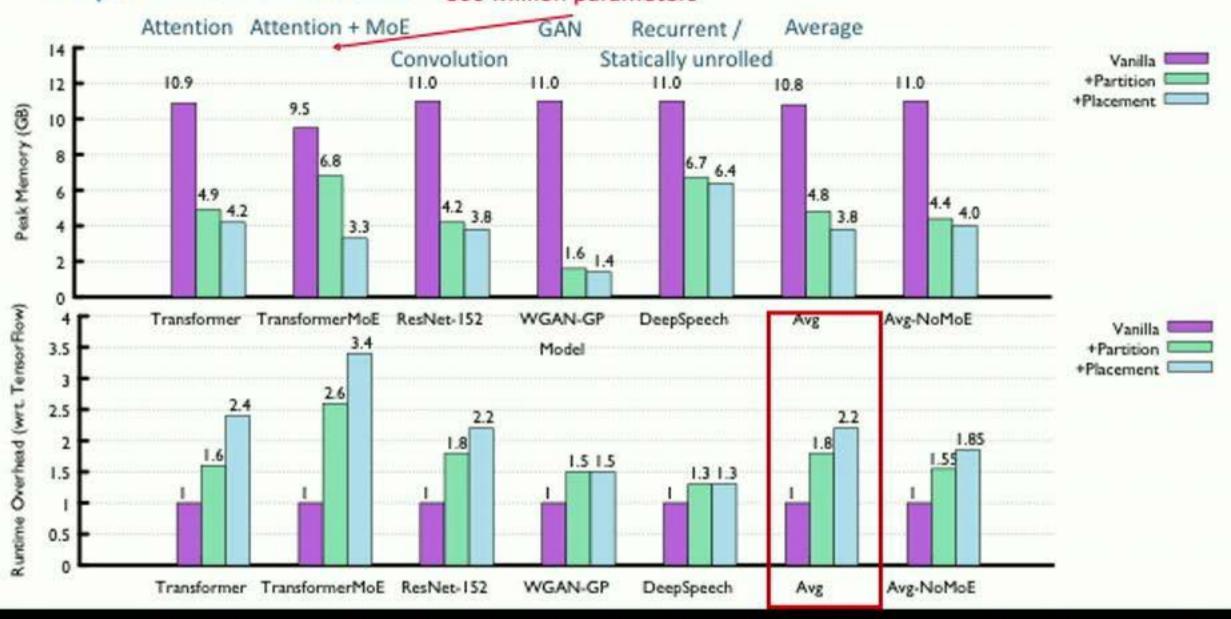
Avg-NoMoE

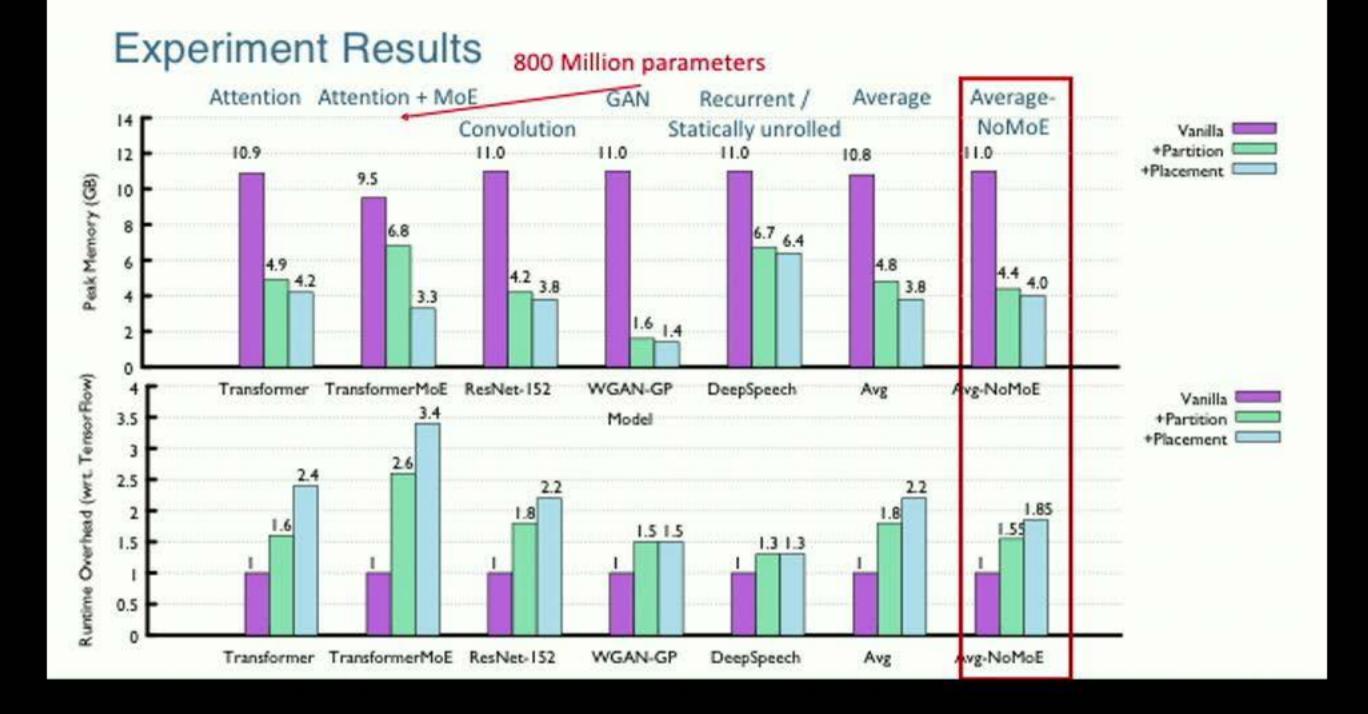
ransformerMoE

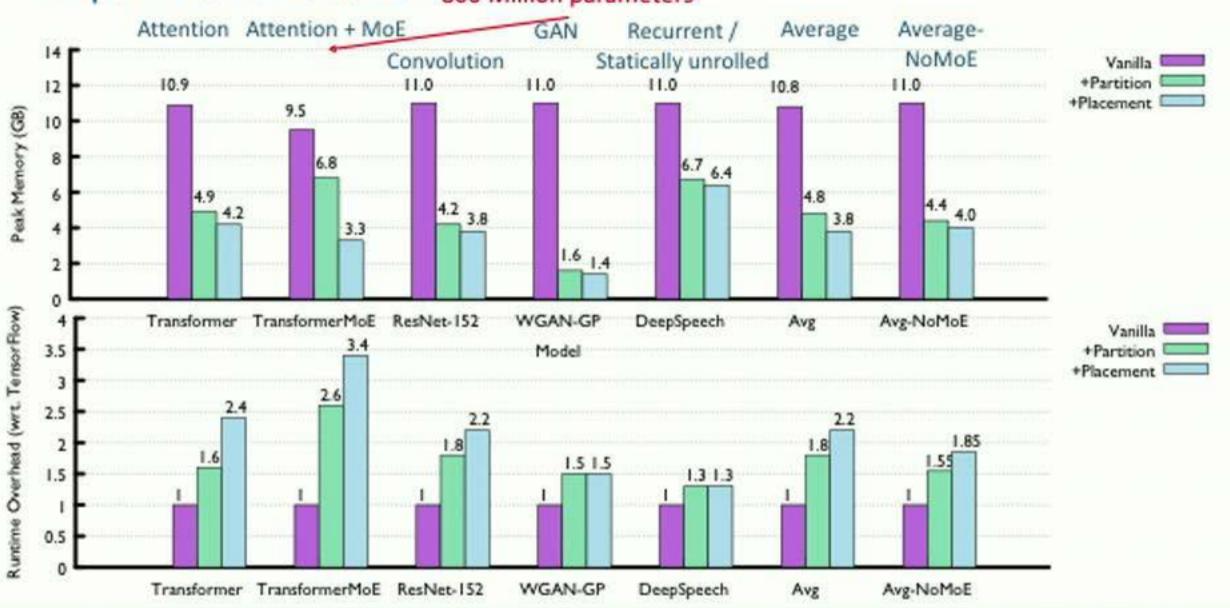
ResNet-152

Transformer









System	#Experts / MoE	#Parameters	Throughput
TensorFlow	4	0.24 Billion	19.0
TensorFlowMem	48	2.5 Billion	1.9

Transformer w/ MoE 12 MoEs, 4M parameters per expert

System	#Experts / MoE	#Parameters	Throughput	Batch	TensorFlow	TensorFlowMem
TensorFlow	4	0.24 Billion	19.0	16	504	1916
TensorFlowMem	48	2.5 Billion	1.9	32	235	1001

Transformer w/ MoE 12 MoEs, 4M parameters per expert Maximum ResNet Depth

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Transformer w/ MoE 12 MoEs, 4M parameters per expert Maximum ResNet Depth

System	#Machines	#Experts / MoE	#Parameters
TensorFlow	4	128	3 Billion
TensorFlow	16	208	5 Billion
TensorFlowMem	4	256	6 Billion
TensorFlowMem + Optimized MoE	4	512	12 Billion

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Maximum ResNet Depth

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TensorFlowMem	48	2.5 Billion	1.9	32	235	1001

#### Transformer w/ MoE 12 MoEs, 4M parameters per expert

Maximum ResNet Depth

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TensorFlow	4	128	3 Billion
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Distributed Transformer w/ MoE 12 MoEs, 2M parameters per expert

Partition big tensors

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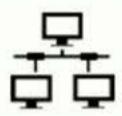
# Recurrent Neural Networks -Scaling Sequence Length

Sequence Length	100	200	400	500	800
TensorFlow	1.15	2.31	4.65	ООМ	ООМ
TensorFlowMem	1.56	3.03	6.03	N/A	12.01

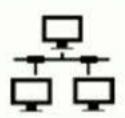
Mozilla DeepSpeech, statically unrolled RNN

Mini-batch size = 128

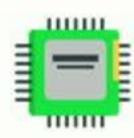
Time per mini-batch (seconds)



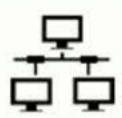
Fine-grained communication
Prioritization based on relative magnitude
Prioritization based on when values are used



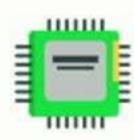
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Statically analyze memory accesses
Schedule independent computation in parallel



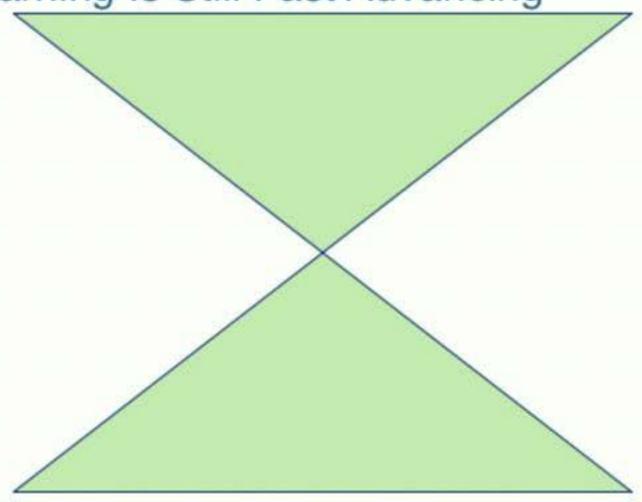
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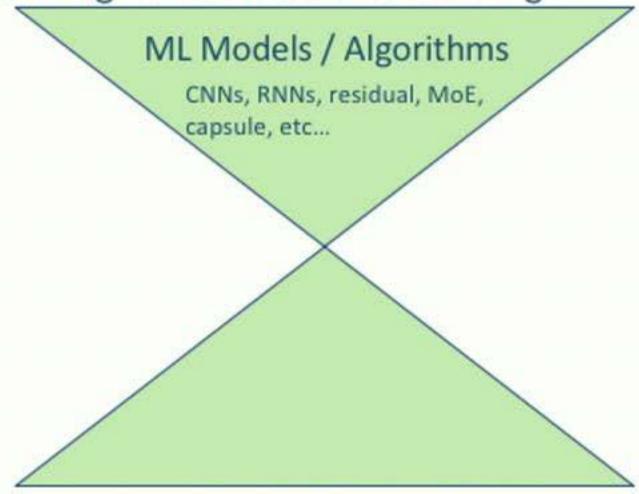


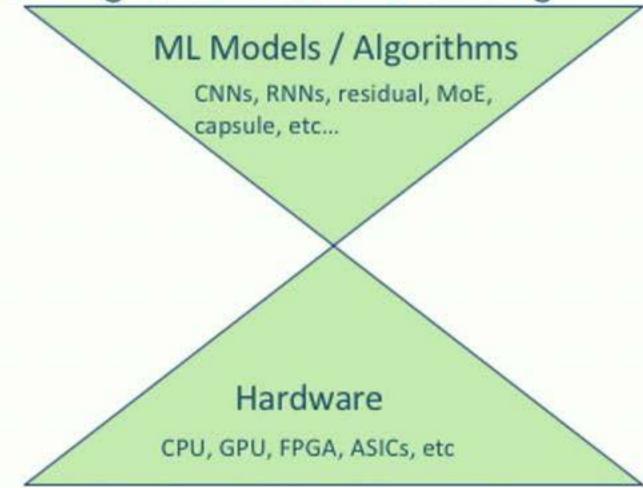
Statically analyze memory accesses
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Partitioned computation graph Leverage cheap host memory







ML Models / Algorithms

CNNs, RNNs, residual, MoE, capsule, etc...

Systems for ML pushing the boundaries of many CS disciplines

Hardware

CPU, GPU, FPGA, ASICs, etc

Machine Learning Is Still Fast Advancing

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HPC

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How to support the expanding ML computation?

How to take advantage of new hardware?

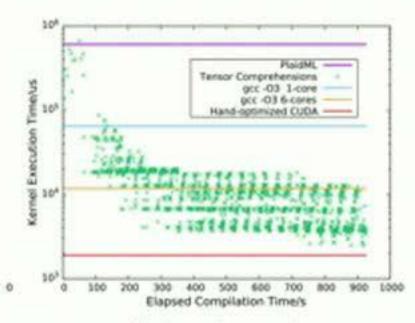
Programming support and compilation

## Programming support and compilation

New operations, e.g., capsule?

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(c) Capsule Kernel

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#### ML-driven optimizations for ML systems

Complex design space

Many ways to reduce memory consumption, with different trade-offs

Many ways to reduce memory consumption, with different trade-offs

**Techniques** 

Trade-off

Many ways to reduce memory consumption, with different trade-offs

Techniques

Trade-off

Scheduling

Degree of Parallelism

Many ways to reduce memory consumption, with different trade-offs

Techniques Trade-off

Scheduling Degree of Parallelism

Gradient checkpointing & Constant folding Computation

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Quantization Accuracy

#### Challenges:

- 1) Scheduling is NP-complete;
- Best configuration depends on the program and hardware;
- 3) Techniques are inter-dependent

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