10 kHz. The video signal and the corresponding modulated rf output (Fig. 2) have a differential phase error of less than 2° and differential gain distortions of 5% to 7%.

The fm system is designed specifically for the TV intercarrier frequency of 4.5 MHz for the U. S. and 5.5 MHz for Europe. The fm system's output from pin 2 is high in harmonic content, so instead is taken from pin 3. This choice sacrifices some source impedance but produces a clean fundamental output, with harmonics decreased by more than 40 dB.

The center frequency of the oscillator has approximately the same resonance as $L_2$ and the effective capacitance from pin 3 to ground. In addition, by keeping the reactance of the inductor at a point between 300 and 1,000 Ω, the overall stability of the oscillator is ensured.

Optional biasing of the audio-input pin (14) at 2.6 to 2.7 V dc reduces harmonic distortion by about 2 to 1. A separate oscillator power supply (pin 4) permits the sound system to be disabled while the a-m section is being aligned.

The modulator circuit has channel 3 and 4 bandswitching, video synchronous tip clamping, and audio biasing to reduce distortion further. The value of $R_6$ permits the intercarrier amplitude to be adjusted easily with the minimum of rf oscillator coupling to pin 1. With a 12-V regulated power supply, there is less than ±10-kHz shift of rf carrier frequency from 0° to 50°C for any video input level. □

# OTA multiplier converts to two-quadrant divider

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An inexpensive two-quadrant divider that is useful in tunable and tracking filters and special-purpose modulators and demodulators may be built using an operational transconductance amplifier (see figure). This circuit is based upon a multiplier circuit by W. G. Jung[1].

The desired circuit response is achieved by placing the CA3080 multiplier within the feedback loop of the 308 comparator. This method implements the divider function more easily than—and just as accurately as—the logarithmic and antilog converters often employed.

The transfer function of the circuit is given by:

$$V_{out}/V_{in} = -(1+k)/kR_2g_m = -[2(1+k)V_T/kR_2I_B]$$

where k = the resistance scaling ratio and $g_m^* = I_B/2V_T$ for the CA3080. $V_T$ is the thermal voltage (26 millivolts at 23°C). The divider gain is thus inversely proportional to the input bias current, $I_B$. The plot in the figure shows the divider's nearly ideal response. Gain measurements were made with a selective voltmeter having a bandwidth of 10 hertz (HP 3581C) to eliminate noise effects—the circuit's linearity extends over five decades.

The offset of the 308 is also amplified as the circuit's bias current is reduced. Thus, $I_B$'s lower limit should be around 20 nanoamperes. Also, the compensating capacitor must be at least equal to $A_{max} \times 30$ picofarads, where $A_{max}$ is the maximum attenuation given by the divider circuit. The circuit uses a 300-pF capacitor because the maxiumum attenuation is 20 decibels.

The circuit's response to temperature variations is minimal, but in critical applications compensation is necessary for $V_T$. A temperature-compensating resistor having a thermal coefficient of 0.33% per °C for the resistor value $kR_1$ is used in this instance. □

**References**
1. W. G. Jung, "Get gain control of 80 to 100 dB," Electronic Design, June 21, 1974, pp. 94–99.

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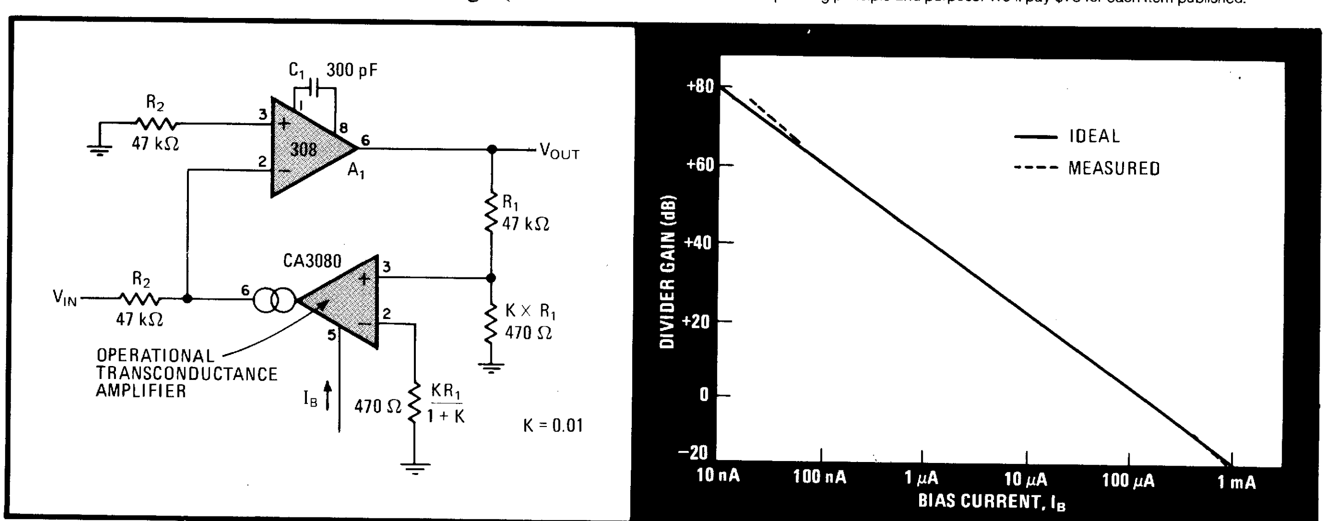


**Inverse.** A basic two-chip multiplier is easily transformed into a two-quadrant divider by the appropriate feedback. This scheme is simpler, no less accurate, and less costly than those using log and antilog converters. Circuit linearity extends to five decades of control current, $I_B$. Except for the most critical applications, temperature compensation is not required.